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A Fuzzy Controlled Single-Stage Integrated Double Buck AC/DC Converter for Power Led Lamps

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Abstract: *In this paper an integrated single stage-single single switch AC-DC converter is proposed which act as a high power factor driver for power LED lamps. The circuit ensures a stable source of supply and good efficiency for the lamp. The converter is operated in discontinuous conduction mode and depending on the output power ratings, the power stage to drive an LED can be classified in to single-stage and two-stage structures. The single-stage structure is for low-power LED lighting applications is used in this paper. The control method used in circuit is the fuzzy logic control which has inherent merits of flexibility and ease in design. The proposed converter provides high efficiency, high PF, low total harmonic distortion even when the output power is very low and the absence of transformer reduces the cost and complexity of the converter.*

Keywords: *Double Buck, Fuzzy Logic Controller, Power factor correction, LED Lamp, Transformer-less, Single Stage, Single Switch.*

I. Introduction

LED technology has experienced an exciting development in recent years. It is commonly accepted as a new generation of light source for its energy saving, because of its high luminous efficacy, ease to drive, absence of a mercury problem and long lifetime. White power LED's offer a promising substitution against energy inefficient incandescent lamps and fluorescent lamps. Thus LED's are expected to override fluorescent and other discharge lamps in many applications like street lighting, house hold applications, automotive lighting, decorative applications etc [1]-[2].

In this paper, an integrated double buck AC-DC converter is proposed as a driver circuit for power LED lamps for providing high power factor, low output current ripple and good efficiency. Single-Stage (SS) high-power-factor (HPF) integrated converters have proven to be a good solution to implement power supplies that comply with harmonic regulations such as the IEC 61000-3-2 [3]–[6].

SS converters integrate a buck PFC cell followed by a DC-DC cell, and use a bulk capacitor between them to attain fast output voltage regulation. The SS converter can operate either in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). The operation in CCM offers the advantage of requiring lower root mean- square (rms) currents through the power switches, which yields high efficiency. However, operation in CCM presents the disadvantage of having no relationship between the output power and the duty cycle of the control switch. This finally causes a high bulk capacitor voltage at low output power levels. This is an important disadvantage especially when a universal input voltage range is pursued.

The other possibility is the operation of a single stage dc–dc converter in DCM. In this case, the output power will depend on the duty cycle of the control switch. The operation with both inductors of the PFC cell and dc–dc converter in DCM is particularly interesting. In this case, the ratio between bulk capacitor voltage and the peak line voltage will depend only on the two inductances ratio, being independent of the output power. This means that a reasonable bulk capacitor voltage can be maintained for the universal input voltage range (90 -270 Vrms). Besides, a high bulk capacitance is not necessary, since the voltage ripple across this capacitor, at double line frequency, can be compensated by closed-loop operation. Therefore, the changes on the duty cycle will affect only the output voltage, thus making it possible for a fast output voltage regulation [7]. In order to improve the speed of response of converter, Fuzzy Logic Controller (FLC) is used rather than Proportional Integral (PI) controller [8]-[9].

II. Proposed Converter

The schematic diagram of the IBuBu converter is shown in fig 1. The working of Single Stage Single Switch double buck converter topology is explained by discussing the various modes of operation of the converter. There are six modes of operation for the S2 double buck converter. The characteristic waveforms are also shown. The understanding of different modes of operation will help to analyze the nature of current and voltage waveforms of various components in the converter.

The proposed IBuBuBo converter, which consists of the merging of a buck PFC cell (L_1 , D_1 ,D_a, C_o , and C_b) and a buck dc/dc cell (L_2 , S_1 , D_2 , D_a , C_o , and C_B).. Both cells are operated in discontinuous conduction mode (DCM) so there are no currents in both inductors L_1 and L_2 at the beginning of each switching cycle t_0.

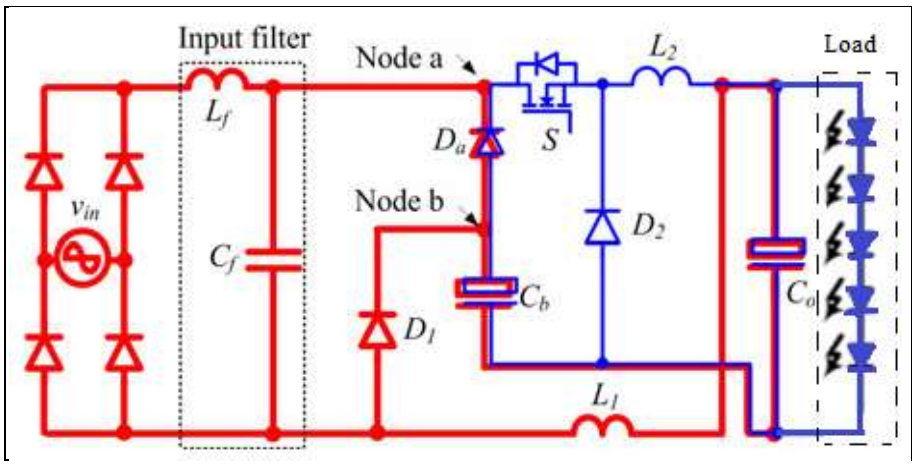


Fig 1. Circuit diagram of an IBUBU converter

Due to the characteristic of buck PFC cell, there are two operating modes in the circuit. The proposed converter includes a buck-type PFC cell, therefore, two working regions can be found within half of line cycle period, as shown in Fig. 2. With the proposed integration, the equivalent voltage Veq = Vb−Vo acts as the sink of the PFC cell, the rectifier does not conduct when vg (θ) < Veq , this interval is defined as Region I. Oppositely, if vg (θ) > Veq , the rectifier conducts and a input current i_{in} appears. This interval is defined as Region II.

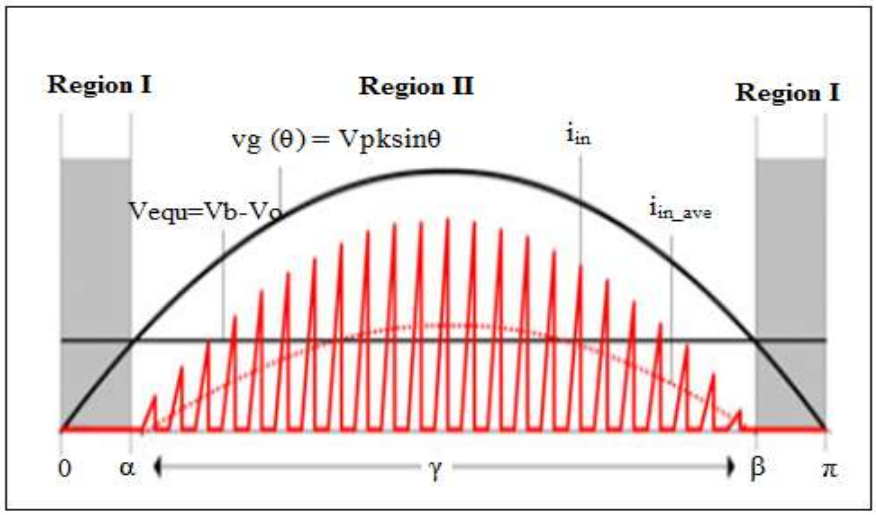


Fig 2.Input voltage and current waveform

2.1. Definitions of Region I and Region II

To simplify the analysis, all components are treated as ideal; the dc link and output capacitors are large enough, therefore their voltage Vb and Vo are treated as constant within half of line-cycle period and after the rectifier, the input voltage *v*in has been rectified as vg (θ) = |vin| = |Vpksinθ|, where Vpk is the peak voltage of vin, and θ is a variable value from 0 to 2π. Especially, considering half of line-cycle from 0 to π, vg (θ) can be expressed as

$$vg(\theta) = |vin| = Vpk\sin\theta \quad \theta \in [0, \pi] \qquad (1)$$

The start point α and end point β of Region II have been marked in Fig. 2 can be expressed as

$$\alpha = \arcsin(V_{equ} \div V_{pk})$$
$$\beta = \pi - \alpha = \pi - \arcsin(V_{equ} \div V_{pk}) \qquad (2)$$

2.2. Operational Modes in Region I

The circuit operation over a switching period can be divided into three stages and the corresponding sequence is Fig. 3 (a), 3 (b) and 3 (c). The key waveforms are shown in Fig. 4.

M1 (t_0− **t_1**) (period M1 in Fig. 4) [see Fig. 3(a)]:

Switch S_1 is turned ON, the voltage applied on L_2 is Veq = Vb−Vo, iL_2 increases linearly from zero with the slope Veq /L_2 ; on the other hand, the voltage applied on the rectifier diodes is vg (θ)−Veq . Noticing vg (θ) < Veq in this region, the rectifier is blocked, there is no current flowing through L_1, $i_{L1} = i_{in} = 0$. This mode will persist until S is turned OFF at t_1. Denoting the duty-cycle as d, the peak value of iL_2 at t_1 can be calculated as

$$I_{L2\_pk} = \frac{V_{eq}}{L2} dTs \qquad (3)$$

Since i_{L2} also flows through S_1 and Cb , the peak values of iC_b and i_S are also $I_{L2-pk.}$

M2(t_1− **t_2**) (period M2 in Fig. 4) [see Fig. 3(b)]:

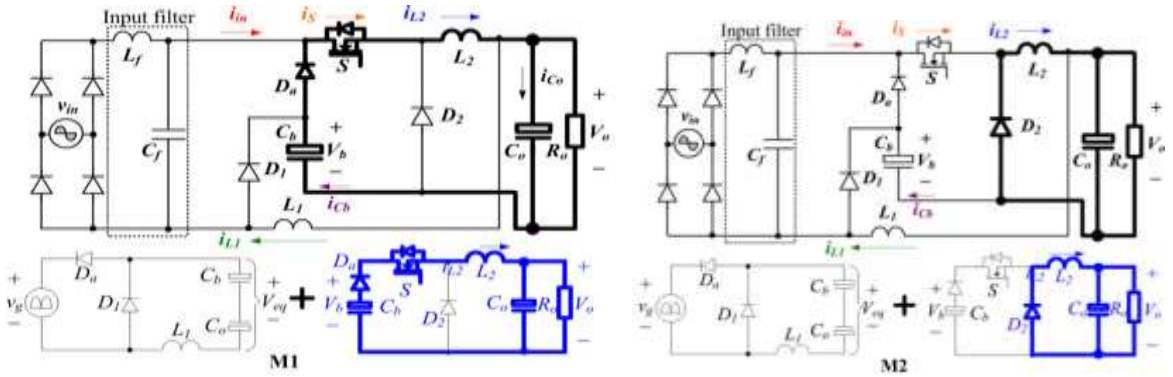
Switch S_1 is turned OFF, iL_2 is freewheeling through S_2 (since S2 is turned on), i_{L2} decreases linearly with the slope Vo /L_2. The current flowing through Cb and S is now zero; in the PFC cell, i_{L1} and i_{in} are also zero, which is the same as M1. This mode will persist until iL_2 decreases to zero at t_2.

Denoting the duty cycle in this mode as d_{DC}, it can be solved as

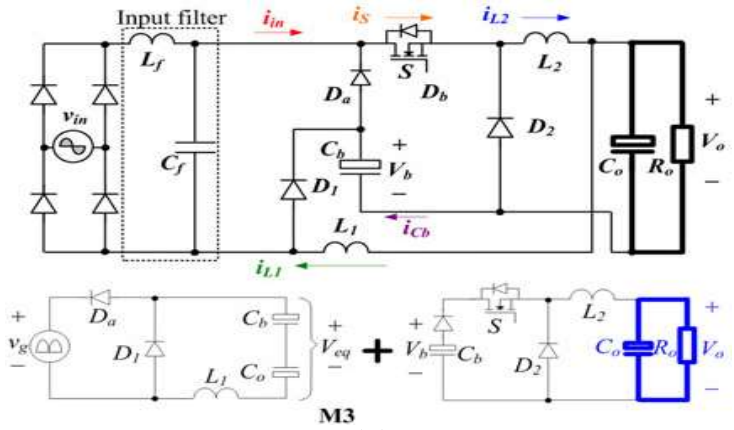
$$d_{DC} = \frac{V_{eq}}{Vo} d \qquad (4)$$

M3(t_2 − t3) (period M3 in Fig. 4) [see Fig. 3(c)]:

Once iL2 decreases to zero, it keeps zero until S is turned ON again. In this mode, only the energy in Co is released to Ro, the currents flowing through L_1, L_2, Cb , and S are all zero. Obviously, the dc–dc cell is actually a buck converter working in the DCM, while the PFC cell is deactivated during this region.



(a) (b)



(c)

Fig. 3 Circuit operation stages of region II of the proposed ac/dc converter

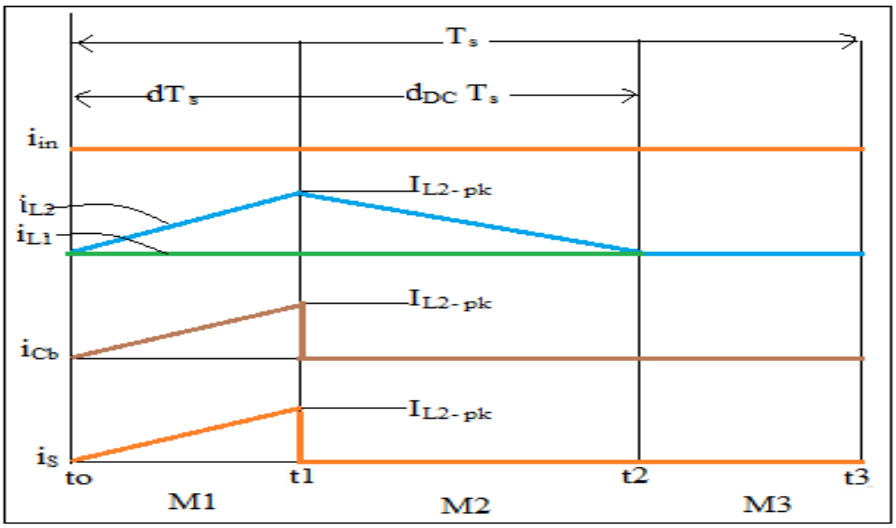


Fig.4. Key waveforms of the proposed circuit in region II

2.3. Operational Modes in Region II

M1(t_0–t_1) (period M1 in Fig. 6) [see Fig. 5(a)]

When S is turned ON in this case, the voltage across L2 is Veq = Vb−Vo, which is the same as that in M1. And since D_a also conducts, nodes a and b have the same voltage levels, it means the voltage applied on L_1 is vg (θ)−Veq. Noticing vg (θ) > Veq, the rectifier is conducted and iL_1 begins to increase linearly from zero with the slope [vg (θ) − Veq]/L1. It should be emphasized that, this mode is persisting only when D_a is conducting. It means $i_S > i_{in}$, or equivalently $i_{L2} > i_{L1}$ must be satisfied, so that the difference current iD_a can be extracted from Cb through Da , and thus, keeps Da conducting. This restriction is satisfied by the appropriate parameter design. This mode will persist until t_1 when S is turned OFF. At t_1, the peak current I_{L2-pk} and I_{S-pk} are the same as (3), and the peak value of i_{L1} and i_{in} can be calculated as

$$I_{L1\_pk} = I_{in\_pk} = \frac{vg(\theta)-V_{eq}}{L1} dTs \qquad (5)$$

M2 (t_1–t_2) (period M2 in Fig. 6) [see Fig. 5(b)]:

S is turned OFF. In the dc–dc cell, i_{L2} is freewheeling through D_2, the voltage applied on L_2 is −Vo, therefore i_{L2} decreases linearly with the slope −Vo /L2, and finally reaches zero at t2 . The corresponding duty cycle d_{DC} is the same as that in (4). In the PFC cell, i_{L1} is freewheeling through D_1, the voltage applied on L_1 is −Veq, i_{L1} decreases with the slope −Veq /L1. In this mode, i_{in} keeps zero and i_{Cb} always equals to $-i_{L1}$.

M3 (t_2−t_3) (period M3 in Fig. 6 [see Fig. 5(c)]:

i_{L2} has decreased to zero, i_{L1} keeps decreasing because the voltage applied on L_1 is still Veq. i_{L1} will finally reach zero at t3. The corresponding duty cycle d_{PFC} can be solved as

$$d_{PFC} = \frac{vg(\theta) - V_{eq}}{V_{eq}} d \qquad (6)$$

M4 (t_3−t_4) (period M4 in Fig. 6) [see Fig. 5(d)]:

Both i_{L1} and i_{L2} are zero, the circuit state goes to M3, as that in region I. It is seen that the dc–dc cell still works as a buck converter, and the equivalent PFC cell also behaves as a buck PFC, where L_1 is the buck-inductor, Veq = Vb−Vo is the equivalent output, and D_1 is the freewheeling diode. It should be emphasized that, if i_{L1} decreases to zero first, the order of M2 and M3 should be exchanged, however, the expressions of d_{DC} and d_{PFC} are not changed because the two freewheeling currents are completely independent.

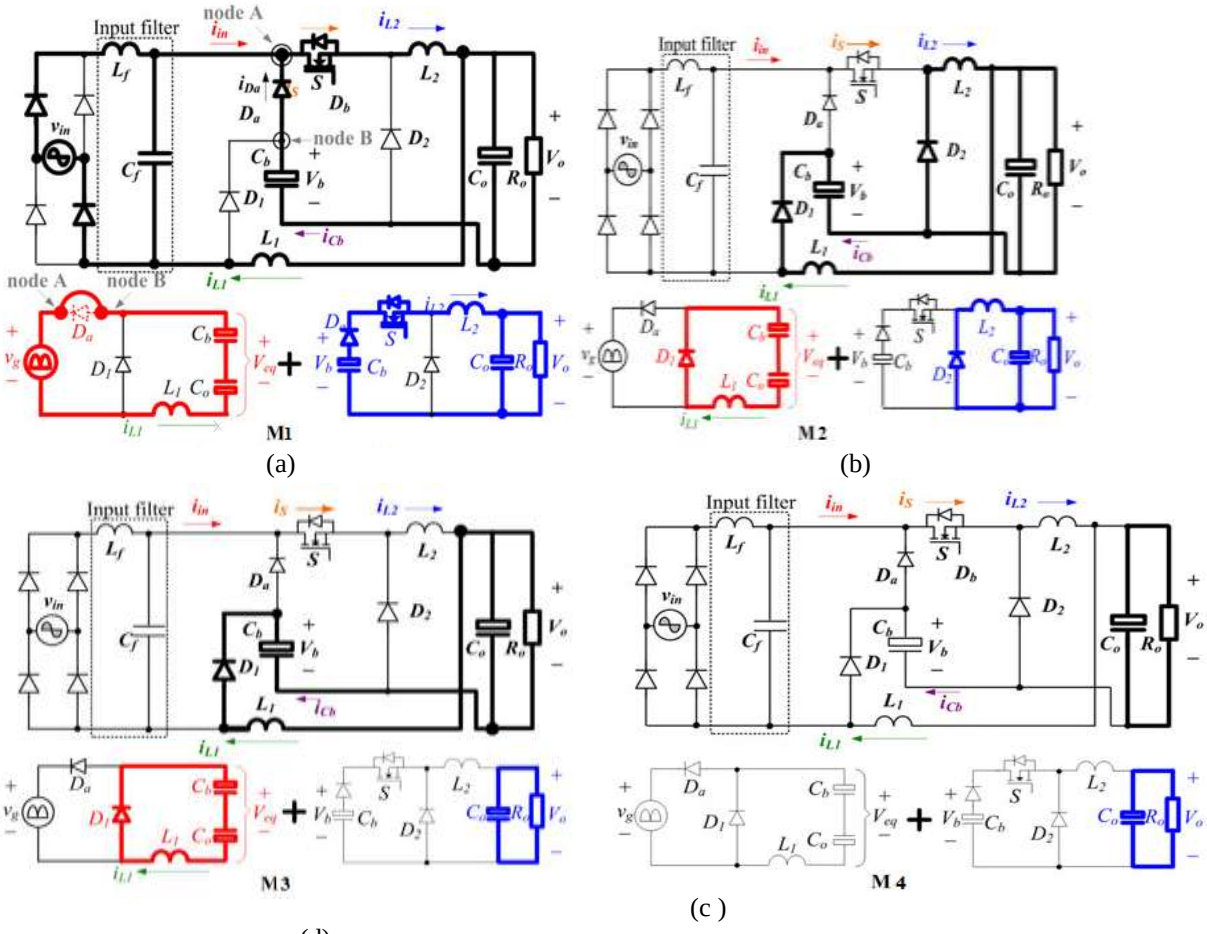


Fig. 5 Circuit operation stages of region II of the proposed ac/dc converter.

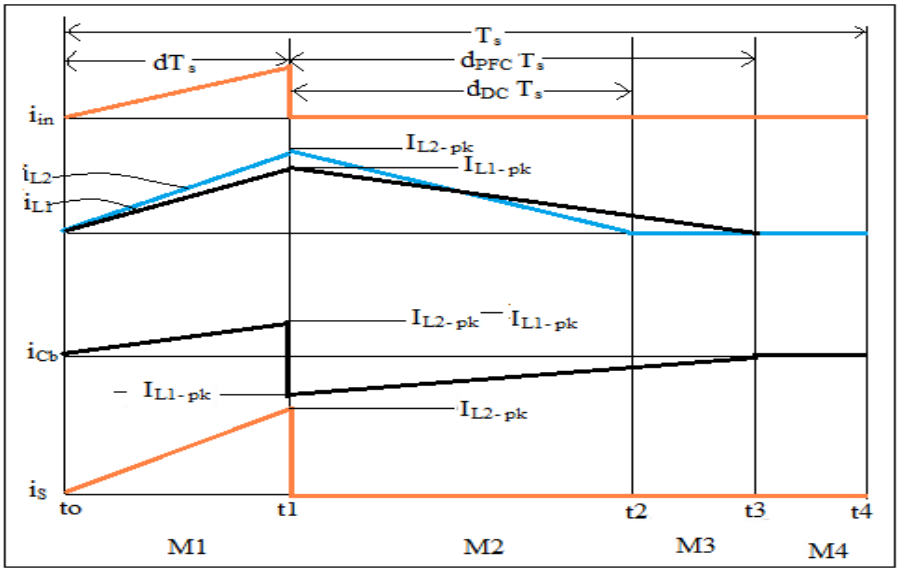


Fig.6. Key waveforms of the proposed circuit in region II

III. Design of Ibubu Converter

The IBuBu converter is designed as follows for simulation in Matlab 2014.
The input voltage of the converter can be varied between (90-270)Vrms.
Let the input voltage be, Vin = 220Vrms
Switching frequency = 20 kHz
Output power = 6W
Switch control = Fuzzy logic control
In order to design the circuit components, first find the Peak-input to equivalent sink ratio Mpe
Mpe = $\frac{Veq}{Vpk}$, where Veq= Vb-Vo
Desired output voltage = 19V, and intermediate bus voltage = 117 V
Veq = 98V
Mpe = .315

a) Calculation of dead angle (α and β) and conduction angle γ

$\alpha = \arcsin(V_{equ} \div V_{pk})$
$= .320$ rad/sec

Similarly,

$\beta = \pi - \alpha = \pi - \arcsin(V_{equ} \div V_{pk})$
$= 2.8211$ rad/sec
$\gamma = \beta - 2\alpha$
$= 2.1811$ rad/sec

b) Calculation of duty ratio

The duty ratio of the IBuBu converter be:

$d < \frac{V_o}{V_o + M_{pe} V_{pk}}$ and
$d < M_{pe}$
$< .16453, < Mpe$

c) Design of inductor

To find the value of inductor, use the following equations

$$L = \frac{2\pi M_{pe}^2}{\pi - 2\arcsin M_{pe} - 2.M_{pe}\sqrt{1-M_{pe}^2}}$$

$$= \frac{2\pi * .2\text{^}2}{\pi - 2\arcsin * .2 - 2 * .2\sqrt{1-.2\text{^}2}}$$

$$= .327666H$$

To find L_2,

$$d = \frac{\sqrt{2\ Po\ L_2 f_s}}{M_{pe}\ V_{pk}}$$

$L_2 = (dM_{pe}V_{pk})\text{^}2/ (2*Po*fs)$

$= 1.082$ m H

$L= L_2/L_1$

$L_1 = 3.30$ mH

d) Design of capacitor

The value of bus capacitor (Cb) and output capacitor (Co) can be found out using equation:

$$Cb = \frac{2Po * thold\_up}{Vb_{Max}^2 - Vb_{Min}^2}$$

Where thold_up = α/ω

$Cb = 9.75$ μ F

Similarly,

$$Co = \frac{2Po * thold\_up}{Vo_{Max}^2 - Vo_{Min}^2}$$

$= 3$m F

e) Design of filter inductor and capacitor

$$F = \frac{1}{2\pi\sqrt{LC}}$$

Assume L = 60mH and F = 1KHz

Then C = 0.10 μF

IV. Simulation

The simulation and verification of an ac-dc converter is done in Matlab/simulink. MATLAB is a software package for computation in engineering, science, and applied mathematics. It offers a powerful programming language, excellent graphics, and a wide range of expert knowledge. MATLAB is published by and a trademark of The Math Works, Inc. As compared to other numerically oriented languages like C++ and FORTRAN, MATLAB is much easier to use and comes with a huge standard library.

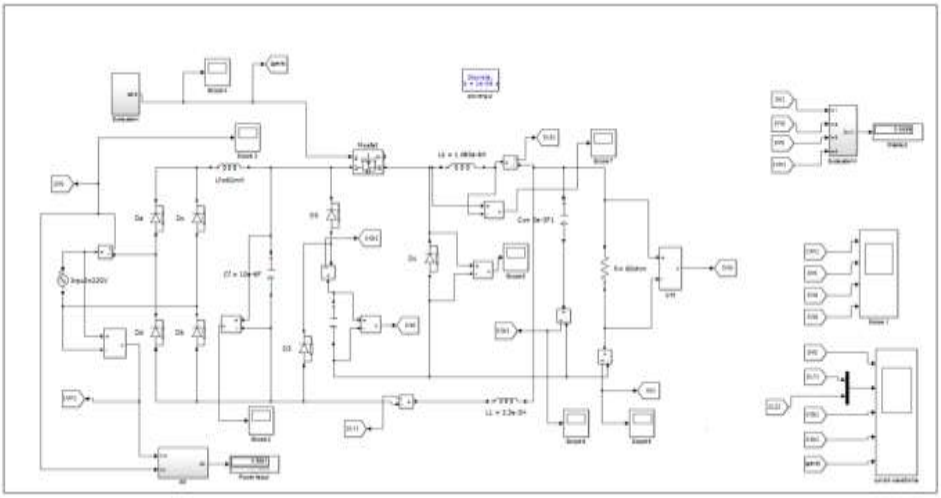


Fig 7.Simulation of proposed converter

In this model there are three subsystem blocks. They are power factor block, efficiency block and controller block. Each block is shown in fig 8, 9 and 10 respectively. From the figure, it is clearly shown that for a given 220V ac input, the output obtained is 19V. This means that a highly step down is occurred without using transformer. High power factor, ie, 0.9709% was automatically obtained by operating the converter in DCM and the efficiency obtained is 86%.

4.1 Subsystems

a) Power Factor Block

Power factor means how effectively the load draws the real power.

Power factor = active power/ apparent power.

In an electric power system, a load with low power factor draws more current than a load with high power factor for the same amount of useful power transfer. So it is often desirable to maintain the power factor of the system nearer to unity.

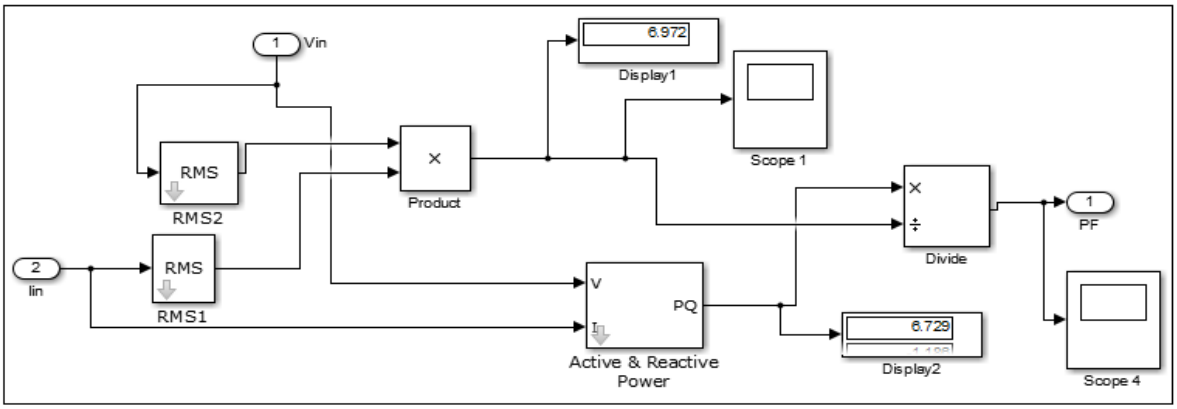


Fig 8 Block diagram for calculating power factor

b) Efficiency block

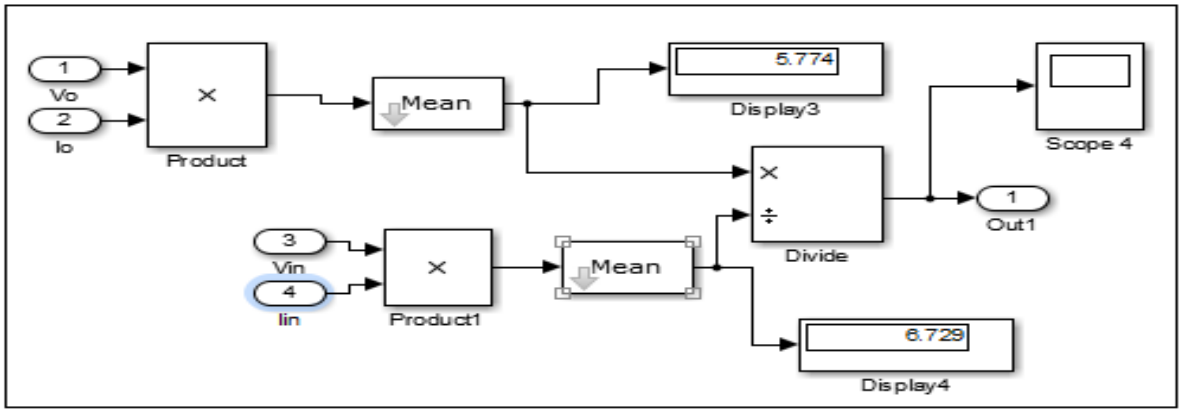


Fig 9 Block diagram for calculating efficiency

c) Fuzzy Logic controller

Figure 10 shows the simulation block of fuzzy logic controller. The two inputs to the fuzzy controller are:

1. Error = Vref- Vo
2. Delta error (change in error) = Present error- Previous error

These inputs are fuzzified, evaluated based on the rules defined and defuzzified by Mamdani FIS to produce the output. Details of fuzzy logic are explained in the next section.

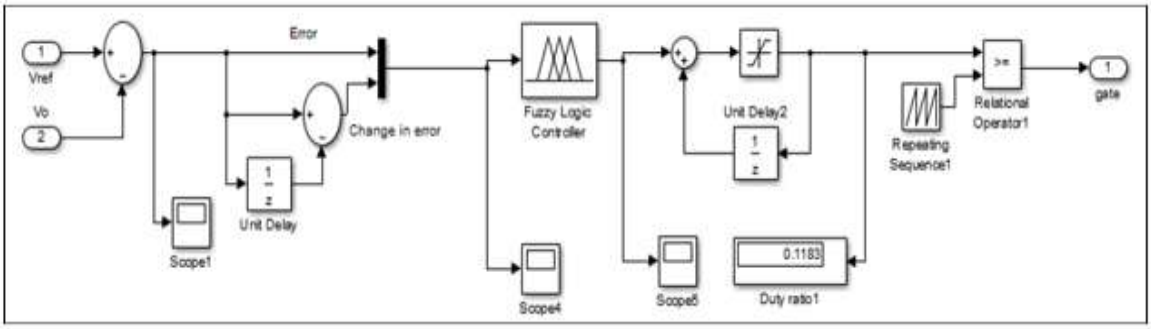


Fig 10 Block diagram of fuzzy logic controller

Fuzzy logic has been an emerging technology since the late 1980s. This is largely because fuzzy controllers have been successfully implemented in application ranging from consumer products, to industrial process control, to automotive applications. Fuzzy logic is simpler than conventional logical systems as it uses an imprecise but very descriptive language to deal with input data more like a human operator. In classical control theory, mathematical models are built which describes the physical plant under consideration. The essence of fuzzy control is to build a model of human expert which is capable of controlling the plant without thinking in terms of mathematical models. Fuzzy systems are advantageous: (a) in situations involving highly complex systems whose behaviors are not well understood and (b) in situations where an approximate, but fast, solution is essential. Fuzzy logic is presented not as a control methodology, but as a way of processing data by allowing partial set membership rather than crisp set membership or non-membership. Fuzzy logic incorporates a simple, rule-based n "If X and Y then Z" approach to solving a control problem rather than attempting to model a system mathematically.

The fuzzy control system is shown in fig 11.

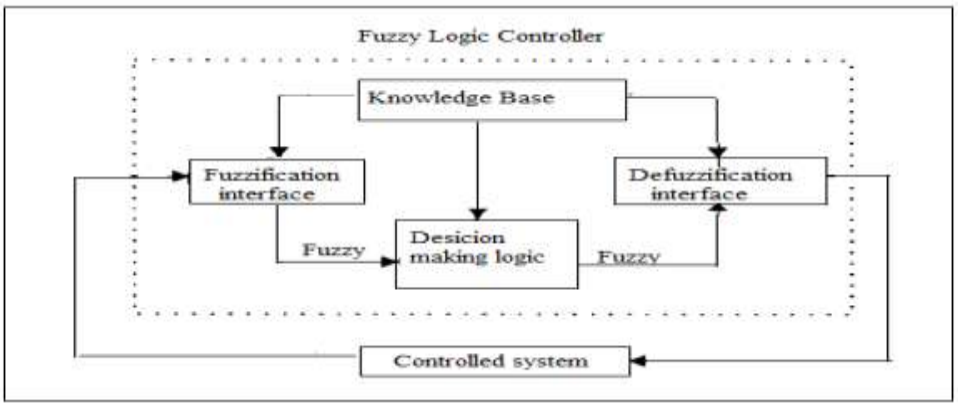


Fig 11 Fuzzy control system

1. Fuzzifier/Fuzzification

Fuzzy logic requires some numerical parameters in order to operate and they are "significant error" and "significant rate-of-change-of-error", but the exact values of these numbers are usually not critical unless very responsive performance is required in which case empirical tuning would determine them. In the fuzzy logic controller mentioned here, we give two inputs to the fuzzy controller, which are

1) Error = Vref- Vo
2) Delta error = rate of change or error

The aim is to obtain desired output voltage by continuously varying the duty cycle of the switch until the desired output is reached. The duty ratio of the switch should increase if the error is high and the duty ratio should decrease if the error is small. When errors become zero, output will be equal to the desired voltage. The input given to a fuzzy controller is a crisp value which needs to be fuzzified by fuzzifier. The fuzzifier converts the crisp input in to fuzzy sets using the membership functions stored in the fuzzy knowledge base. The fuzzy set, are functions that map a value that might be a member of the set to a number between zero and one, indicating its actual degree of membership. A degree of zero means that the value is not in the set and a degree

of one means that the value is completely representative of the set. This produces a curve across the members of the set.

Fig 12 shows the membership function of the input "Error" and fig 13 shows the membership functions input "Delta Error".

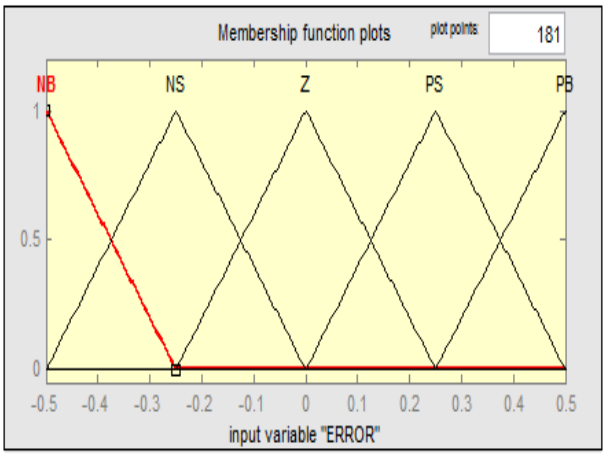


Fig 12 Membership functions of the input "Error"

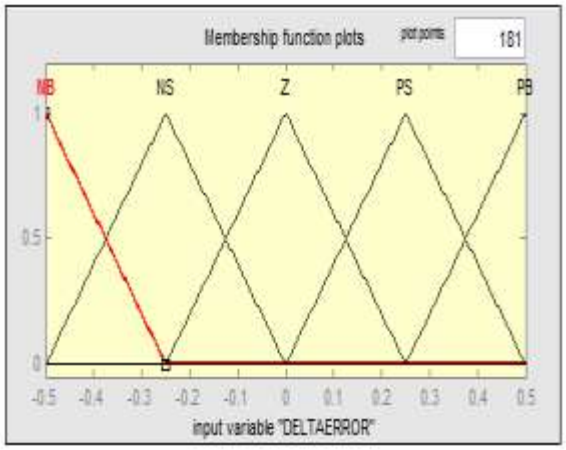


Fig 13 Membership functions of the input "Delta Error"

The input "Error" and "Delta Error" is converted in to five fuzzy sets, using triangular membership function. The membership functions are named as Negative Big (NB), Negative Small (NS), Zero (Z), Positive Small (PS) and Positive Big (PB).

2. Fuzzy Inference System (FIS)

The fuzzy inference engine converts the fuzzy inputs to fuzzy outputs using the "If-Then" type fuzzy rules. There are two types of FIS:

(1) Mamdani
(2) Sugeno

The most fundamental difference between Mamdani-type FIS and Sugeno-type FIS is that the way the crisp output is generated from the fuzzy inputs. While Mamdani-type FIS uses the technique of defuzzification of a fuzzy output, Sugeno-type FIS uses weighted average to compute the crisp output. The Sugeno FIS has better processing time since the weighted average replaces the time consuming defuzzifization process. Due to the interpretable and intuitive nature of the rule base, Mamdani-type FIS is widely used in particular for decision support application.

3. Defuzzifier

Defuzzifier converts the fuzzy output of the interface engine to crisp using membership functions analogous to the ones used by the fuzzifier. Fig 14 shows the membership function defined for the output.

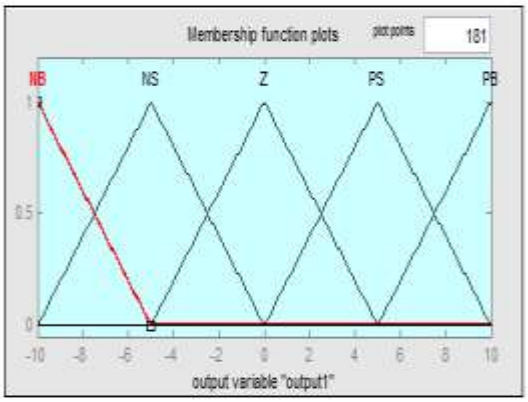


Fig 14 Output Membership functions

4.2 Fuzzy Rules

A fuzzy model consists of a series of conditional and unconditional fuzzy propositions. A proposition or a statement establishes a relationship between a value in the underlying domain and a fuzzy space. A conditional fuzzy proposition is one that is qualified as an "if" statement. The proposition following the "if" term is antecedent or a predicate and is an arbitrary fuzzy proposition. The proposition following the "then" term is the consequent and is also any arbitrary fuzzy proposition.

If w is Z then x is Y

Interpreted as: x is a member of Y to the degree that w is a member of Z

An unconditional fuzzy proposition is one that is not quantified by n "if" statement.

X is Y

Where x is a scalar from the domain and Y is a linguistic variable.

The rules used in the fuzzy controller for proposed converter are shown in table 1 and fig 15

Table 1 Fuzzy rules

Error / Δ Error	NB	NS	Z	PS	PB
NB	NB	NB	NB	NS	Z
NS	NB	NB	NS	Z	PS
Z	NB	NS	Z	PS	PB
PS	NS	Z	PS	PB	PB
PB	Z	PS	PB	PB	PB

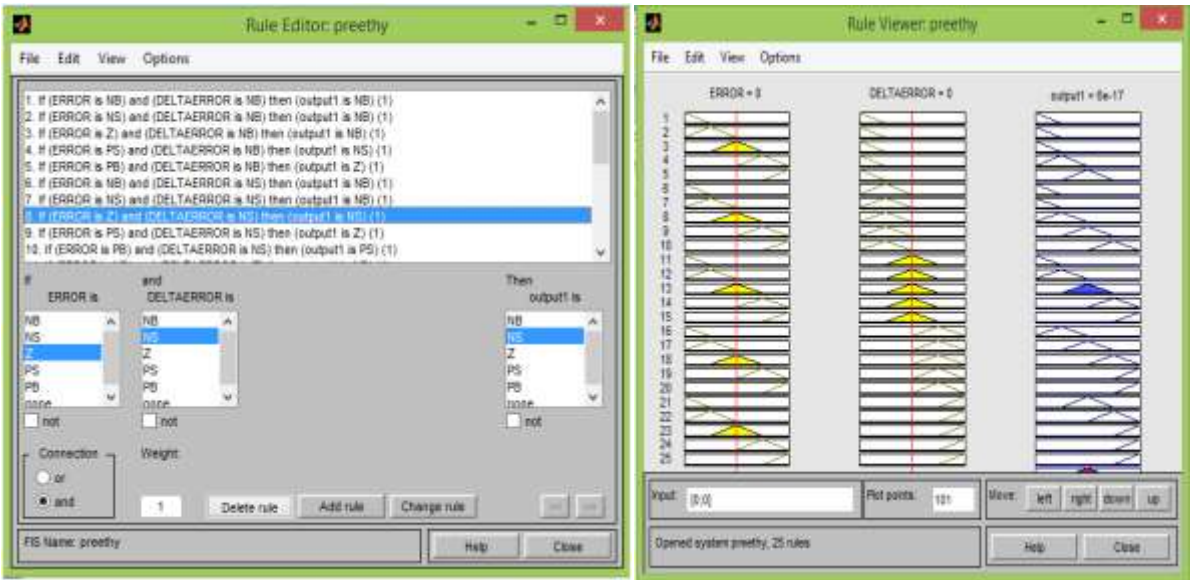


Fig 15 Fuzzy rules

4.3 Simulation Results of the Modified Converter

a) Voltage waveforms

Fig 16 shows the simulation results of input voltage, input current, output voltage and intermediate bus capacitor voltage of the modified converter. From the result, it is shown that for a given 220 V AC input, the output obtained is 19V which is DC and proved the converter is operated in discontinuous conduction mode in entire period. Also the intermediate bus voltage is very much reduced and the value obtained is 117V.

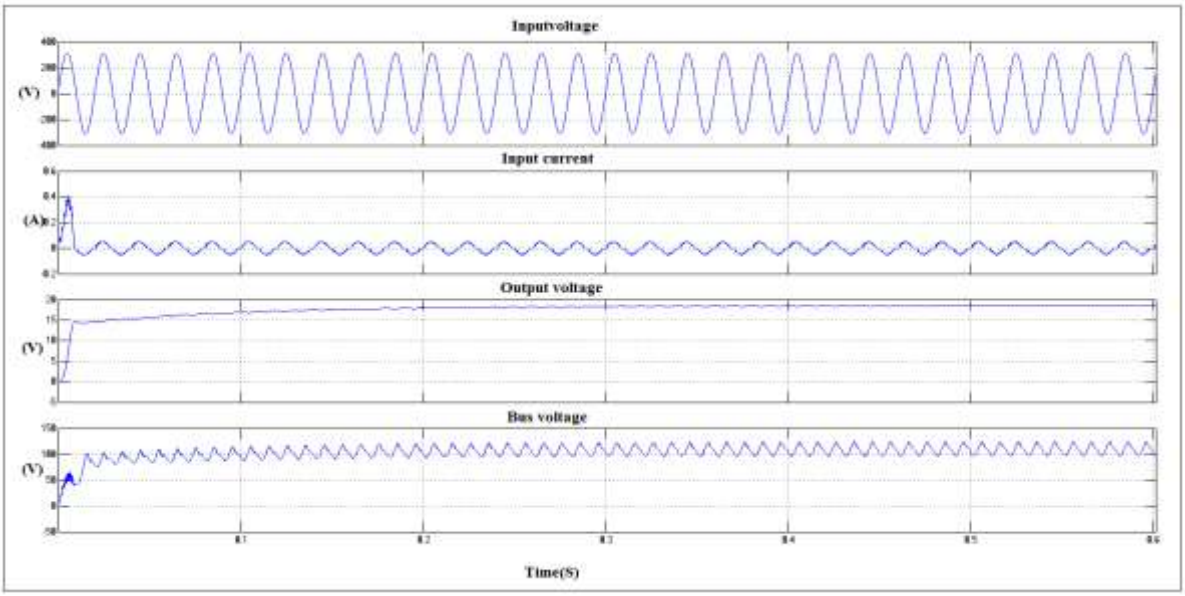


Fig 16 Simulation results of the modified converter

b) Current Waveforms

Current through the main switch (S1), current through the inductors (L1 and L2), Current through the bus capacitor ant the gate pulses of the high side switch and low side switch is shown in fig 17.

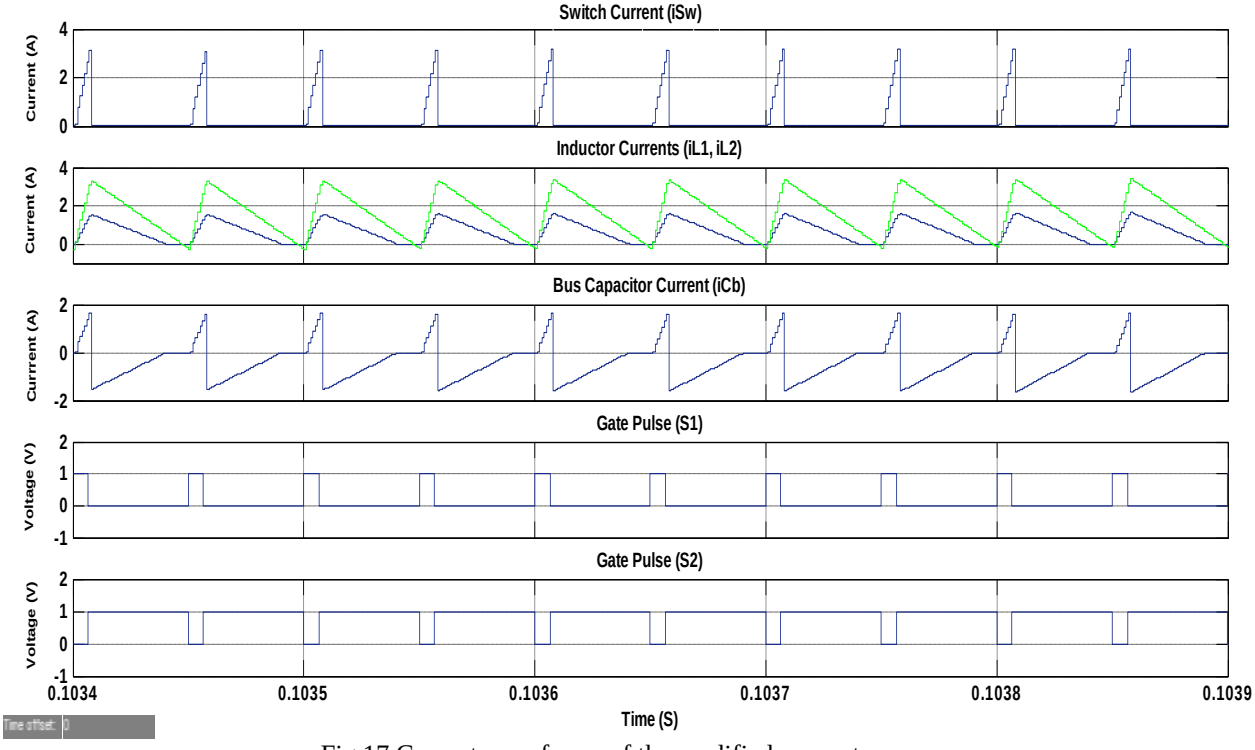


Fig 17 Current waveforms of the modified converter

c) Power Factor

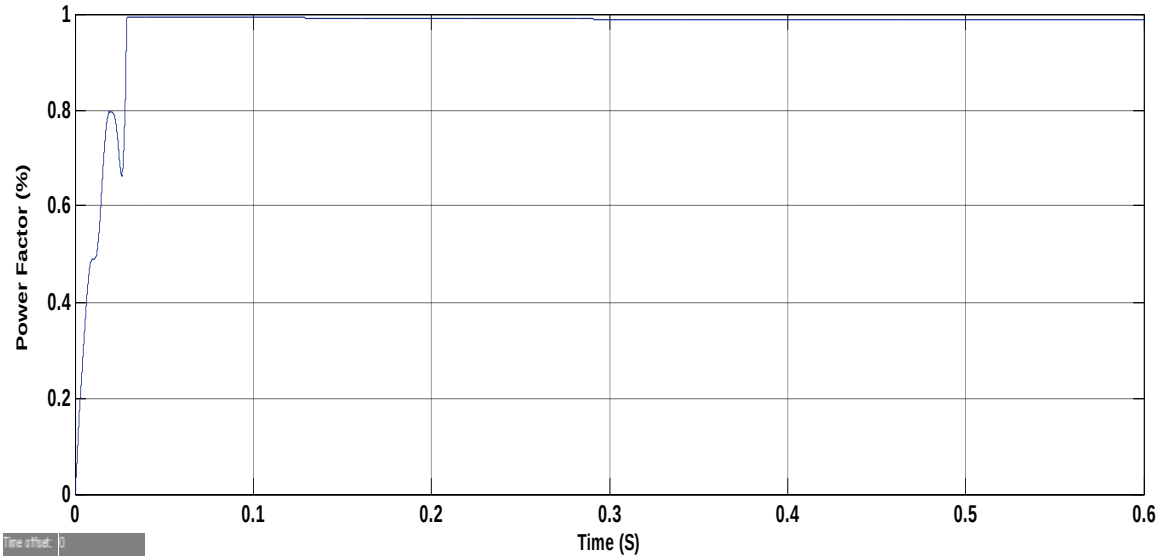


Fig 18 Power factor of the modified converter

As shown the power factor of the modified AC-DC converter is .96. ie, high power factor is automatically achieved by operating the PFC cell in discontinuous conduction mode.

d) Total Harmonic Distortion

To ensure the THD of the input current, IEC61000-3-2 Class C standard is followed in the entire operational range in IBuBu converter. The THD of the proposed converter is 13.53%.

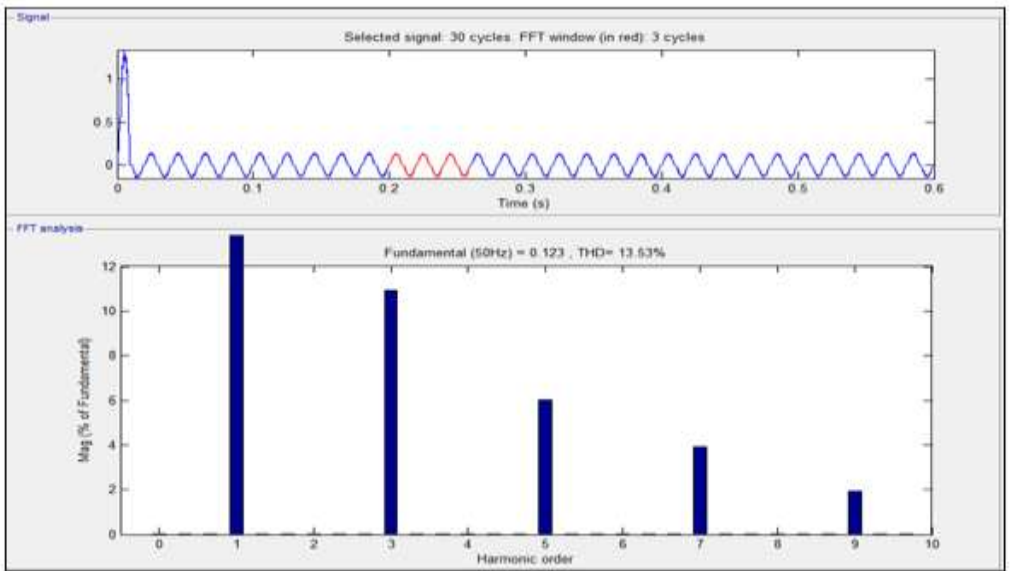


Fig 19 THD of the modified converter

e) Efficiency

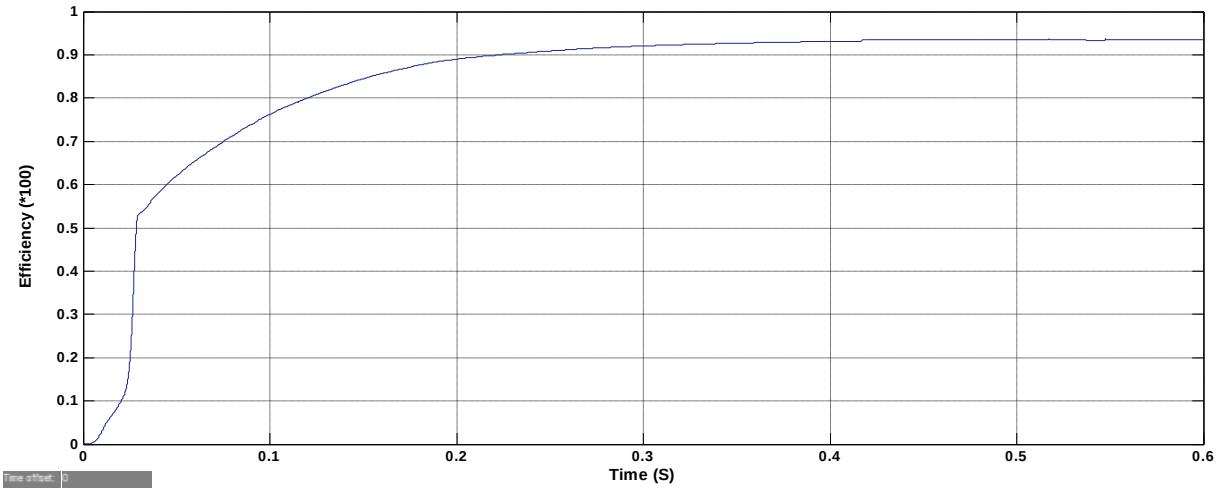


Fig 20 Efficiency of the modified converter

V. Conclusion

This study has helped to understand the fundamental converters used in the electronics industry. An integrated single stage single switch double buck AC-DC converter for LED application using Fuzzzy Logic Control was designed and simulation of the same was done. The proposed IBuBu converter has the following advantages:

1. Due to the integration of two buck cell, a high step-down feature is obtained
2. The buck PFC cell leads to a low dc link capacitor voltage not greater than 160V, voltage stress is low.
3. The switch in the converter needs to handle the current of the DC-DC cell, current stress is low.
4. High power factor and low total harmonic distortion
5. Low cost and small size
6. Replacement of PI controller with fuzzy logic controller improves the speed of response of the converter.

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