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ANALYSIS OF POWER DISSIPATION IN DRIFT REGION OF 6H-SILICON CARBIDE DIMOSFET

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Abstract: *Today we need faster devices with high voltage and high switching frequency capability, generally used Silicon-based devices are not able to meet these requirements as they need costly cooling systems, so we need much faster devices like Wide band-gap based semiconductors. These devices have superior physical properties that offer multiple advantages like lower intrinsic carrier concentration , higher electric breakdown field ,higher thermal conductivity and large saturated electron drift velocity which is suitable for faster devices with high voltage and high switching frequency.*
The paper presents performance difference in terms of current density ,forward voltage ,power dissipation ,power saved between the linearly graded and uniformly doped 6h-sic Dimosfet .The paper also discusses the results of mathematical analysis of power dissipation in the linearly graded and uniformly doped drift regions in SIC. The paper shows that there is significant reduction in power dissipation in the linearly graded profile than the uniformly doped one and this reduction increases with increasing magnitude of current density.

I. INTRODUCTION

SIC is the currently a new device which is being projected as a potential device that can be used for variety of high power and high frequency operations. These include high-power high-voltage switching applications, high temperature electronics, and high power microwave applications in the 1 - 10 GHz regime. SiC is attractive for these applications because of its extreme thermal stability, wide band gap energy, and high breakdown field .Also due to its wide band gap energy(3.0eV and 3.25eV for the 6H and 4H polytypes respectively), leakage currents in SiC are many orders of magnitude lower than in silicon, and the intrinsic temperature is well over 800°C.

These electronic properties make SiC attractive for high temperature electronics applications. Along with this the breakdown field in SiC is around 8times higher than that in silicon. This property is critical for power switching devices, as the specific on-resistance scales inversely as the cube of the breakdown field. Thus, devices made out of SiC are expected to have specific on-resistances 100 – 200 times lower than comparable silicon devices [1]. Lastly, SiC is the only compound semiconductor that can be thermally oxidized to form a high quality native oxide (SiO2). This makes it possible to fabricate MOSFETs, insulated gate bipolar transistors (IGBTs), and MOS-controlled thermistor's (MCTs) in SiC

II. SIC POLYTYPES

Silicon carbide exists in many different polytypes. All polytypes have a hexagonal frame with a carbon atom situated above the center of a triangle of Si atoms and underneath there is a Si atom belonging to the next layer. The difference between the polytypes is the stacking order between succeeding double layers of carbon and silicon atoms [3].

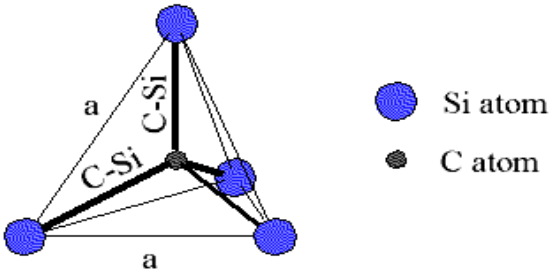


Figure 1.1Tetragonal bonding of a carbon atom with the four nearest silicon neighbors [3].

The fig (1.1) shows the stacking sequence for the three most common polytypes, 3C, 6H and 4H. Here if the first double layer is called the A position, the next layer can be placed according to a closed packed structure that will be placed on the B position or the C position. All the polytypes will be constructed by permutations of these three positions.

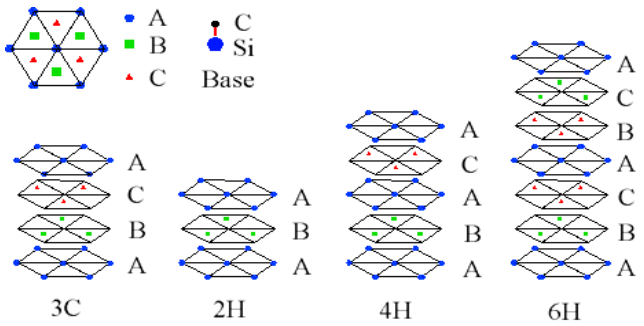


Figure-1.2The stacking sequence of double layer of the three most common SiC polytypes [3].

A comparison can be made in the properties ofSiC,Si and GaAs including all the different polytypes of SiC at room temperature.

TABLE-1.1Comparison of properties of SiC with Si and GaAs at room temperature [4].

Properties	Si	GaAs	6H-SiC	4H-SiC	3C-SiC
Energy Bandgap (eV)	1.1	1.42	3.0	3.2	2.3
Breakdown Field@1017 (MV/cm)	0.6	0.6	3.2	3.0	1.5
ElectronMobility@1016 (cm2/V-	1100	6000	370	800	750
Saturated Electron Drift Velocity (cm/s)	10^7	10^7	$2x10^7$	$2x10^7$	$2.5x10^7$
Thermal Conductivity (W/cm-K)	1.5	0.5	4.9	4.9	5.0
HoleMobility@1016 (cm2/V-s)	420	320	90	115	40

The comparison shows that SiC has a large band gap, which is nearly three times larger than that of silicon and the large Si-C bonding energy makes SiC resistant to chemical attack and radiation .SiC belongs to the category of wide band gap semiconductors, where conventional semiconductors like Si and GaAs cannot adequately perform under extreme conditions. This wider band gap of SiC also enables it to be designed smaller and with higher density that can withstandhigh voltages .Its high thermal conductivity of also decreases the need for special packaging and system cooling for device operation [4].

III. STRUCTURE OF 6H-SiC DIMOS

Fig.2.1 shows a cross section of a power DIMOS structure. Thisstructure is fabricated by using planar diffusion technology with a refractory gate suchas poly-silicon .Here ,the P-base and N+-source regions are diffused through a common window defined by the edge of the poly silicon gate. The surface channel region is defined by the difference in the lateral diffusion between the P-base and N+-source region.

The forward blocking capability is achieved by the PN junction between the P-base region and the N-drift region.During device operation, a fixed potential to the P-base region is established by connecting it to the source metal by a break in the N+ source region. By short circuiting the gate to the source and applying a positive bias to the drain, the P-base/N-drift region junction becomes reverse-biased and this junction supports the drain voltage by the extension of a depletion layer on both sides.

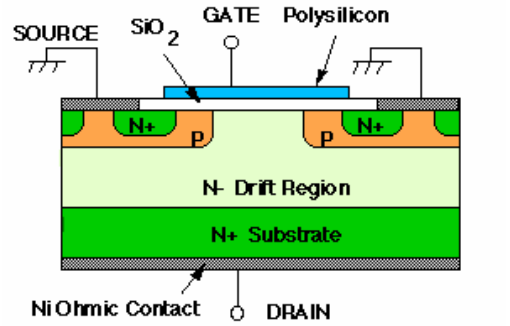


Figure-1.3Cross-section view of DIMOS [5], [7]

IV. MODEL FOR DIMOSFET

The Double Implanted Metal-Oxide Semiconductor (DIMOS) field effect transistor has been frequently used in high voltage power electronics applications. The performance of the device is limited by the quasi-saturation behavior in its characteristics. It is shown that such effect is due to the carrier velocity saturation because of the high electric field, low impurity concentration in drift layer, and narrow pbody spacing. The detail of DIMOS structure identifying different regions of operation isshown in Fig.. Since the diffusion process in 6H-SiC is ineffective, ion implantation is the only way to form p-body and n+ region for the vertical structure and double diffusion is not suitable for the 6H-SiC device fabrications. The n-drift region is usually doped lightly (.5x1014 /cc) to reduce the losses in the drift region. The n+ regions were doped with (.1.5x1020 /cc) Nitrogen; p-body regions were formed with (. 4x1017 /cc) Boron implantations [9].

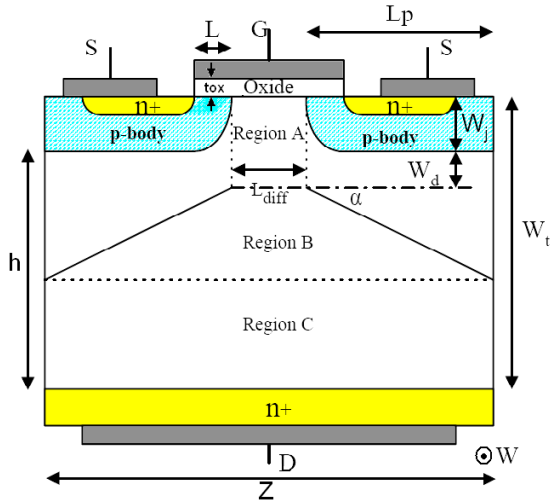


Figure1.4Structure of Double Implanted Metal-Oxide Semiconductor (DIMOS) [9].

hdrift-region height of the device (cm, depends on Vb and doping profile),
W width of the device (cm),
Wjheight of the p-body (cm),
Wt total vertical height (cm),
Wddepletion width (cm),
L channel length formed under the gate and inside the p-body (cm),
Lplength of p-body (cm),
Ldiff separation of p-bodies (cm),
Z total length of the device (cm),
Toxoxide thickness (cm),
VT threshold voltage of the device (volt),
VGS applied gate to source voltage (volt),
Vsatsaturation velocity (cm/sec),
q Electronic charge (C),

αangle of slope of the drift region narrowing (degree),
εopermittivity constant in free space (F/cm),
εoxoxide permittivity (F/cm).
εsicsilicon carbide permittivity (F/cm),
A cross-sectional area of the device (cm^2)

V. CALCULATIONS

The drift region has been divided into three parts: an accumulation region A, a drift region B with varying cross section area, and drift region C with constant cross section. Voltages of these regions are given by [9],

$$V_{A=} \quad \frac{I_d \ (\ W_j + W_d\ )}{W\ (L_{diff} q N_d) \mu_{Neff} - Id/E_c} (1)$$

$$V_B = \frac{I_d}{W\ q\ N_d\ \mu_{Neff}\ \cot\alpha} \log\left[\frac{W\ q\ N_d \mu_{Neff} (L_{diff}+Lp) I_d/Ec}{W\ q\ N_{dLdiff}\ \mu_{Neff}\ - I_d/E_c}\right] (2)$$

$$V_c = \frac{I_d \ (W_t - W_j - W_d - L_p \tan\alpha)}{W\ (L_{diff} + L_{p)}\ q\ N_d\ \mu_{Neff} - I_d/E_c} (3)$$

VI. TABLES AND GRAPHS FOR UNIFORMLY DOPED PROFILE

The table shows the values of current density at different values of doping concentration for uniformly doped profile.

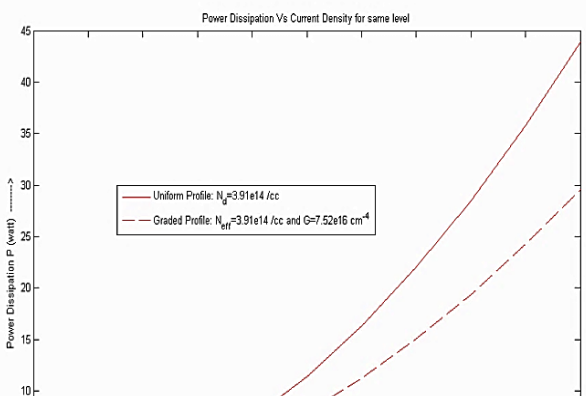
Table1.4:Values of Current Density at different levels of doping for different values of ForwardVoltage

$J_r(A/cm^2)$	V_f(volt) $N_d=3.91e14/cm^3$ $\mu_{Eff}=530cm^2/vsec$	V_f(volt) $N_d=2.15e15/cm^3$ $\mu_{Eff}=450cm^2/vsec$	V_f(volt) $N_d=1.45e17/cm^3$ $\mu_{Eff}=450cm^2/vsec$	V_f(volt) $N_d=1.09e17/cm^3$ $\mu_{Eff}=290cm^2/vsec$
1	0.4103	0.0748	0.0131	2.70e-3
10	4.0724	0.7473	0.1307	0.0270
15	6.0934	1.1204	0.1961	0.0405
20	8.1075	1.4933	0.2614	0.0540
30	12.119	2.2386	0.3921	0.0810
50	20.084	3.7272	0.6533	0.1349

Table-1.5Values of power dissipation at different levels of current density for different values of doping

N_d(/cc)	$\mu_{eff}(cm^2/vsec)$	P(watt) $J_f=1A/cm^2$	P(watt) $J_f=10A/cm^2$	P(watt) $J_f=100A/cm^2$	P(watt) $J_f=1000A/cm^2$
3.91e14	530	4.92e-5	4.89e-3	0.4770	43.888
5.17e14	530	3.73e-5	3.71e-3	0.3639	34.231
8.00e14	530	2.41e-5	240e-3	0.2374	22.848
1.28e15	530	1.51e-6	1.50e-3	0.1493	14.587

The plots of power dissipation, PD versus current density for uniformly doped were obtained.These results were compared with those obtained with linearly graded profile and the graphwas plotted.



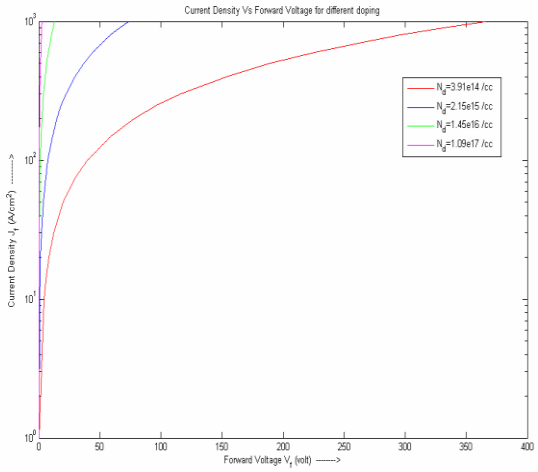


Figure-1.6: The plot shows current density versus forward voltage for various doping levelsFigure-1.7The graph shows the variation of power dissipation.

VII CONCLUSION

The analysis has been done and for a given value of doping level, say 3.91x1014cm-3, shows that the power dissipation is much greater than those of a graded profile with a gradient of 7.52x1016cm-4 and N_{eff}equal to the doping level 3.91x1014cm-3 of the uniformly doped device. The magnitude of Power dissipation with these specifications shows that at a current density of 1000A/cm^2 gives a power dissipation of about 43.88W for a uniformly doped device as against 29.56W for the linearly graded DIMOSFET. There is a decline in Power Dissipation for all values of current density and all values of doping levels in the case of linearly graded device than the uniformly doped one. The graph shows the percentage power saved in linearly graded profile against gradient and effective doping level for different values of current density.

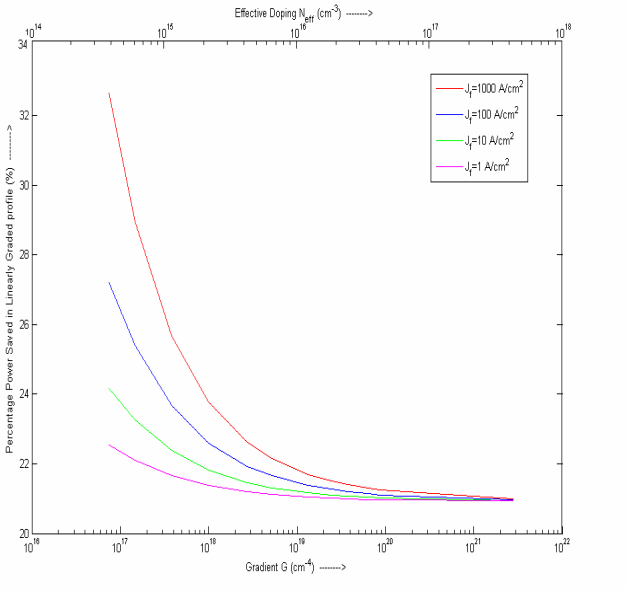


FIGURE-1.8Plot of Percentage Power Saved in Linearly Graded profile against Gradient & Effective doping for different values of current density

In conclusion it may be said that a DIMOSFET with linearly graded drift region can significantly lower power dissipation at high current levels at a given values of effective doping level and concentration gradient as compared to the same doping level of a uniformly doped drift region of a DIMOSFET. The calculations for this device have been made to set the device height of 148.61μm in order to accommodate a blocking voltage of 8kV.

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