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Viterbi Algorithm for error detection and correction

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ABSTRACT: *In the present world, communication has got many applications such as telephonic conversations in which the messages are encoded into the communication channel and then decoding it at the receiver end. During the transfer of message, the data might get corrupted due to lots of disturbances in the communication channel. So it's necessary for the decoder tool to also have function of correcting the error that might occur. Viterbi algorithm has got many applications due to its error detection and correction nature. Convolution encoding with Viterbi decoding is a powerful method for forward error correction. It has been widely deployed in many wireless communication systems to improve the limited capacity of the communication channels. In this project, viterbi algorithm is implemented for detection and correction of single bit error [1].*
Keywords- *Communication, Encoder, Decoding, Convolution coding, Viterbi Algorithm*

I. INTRODUCTION

In communication system, error detection and correction mechanisms are vital and numerous techniques exist for reducing the effect of bit-errors and trying to ensure that the receiver eventually gets an error free version of the packet. The major techniques used are error detection with Automatic Repeat Request (ARQ), Forward Error Correction (FEC) and hybrid forms of ARQ and FEC. This project focuses on FEC techniques. Forward Error Correction (FEC) is an error control method for data transmission by adding redundant data to its messages to improve the capacity of a channel. This redundant data allows receiver to detect and to correct a certain number of errors without asking the encoder to re-transmit more additional data. The process of adding this redundant information is known as channel coding.

Mainly there are two major kinds of channel coding: block codes like Reed –Solomon coding, and Convolutional coding. Block codes work with fixed length blocks of code. Convolutional codes deal with data sequentially. Block codes become very complex as their length increases and are therefore harder to implement. Convolutional codes, in comparison to block codes, are less complex and therefore easier to implement.

I.I GENERIC METHODS FOR DECODING CONVOLUTIONAL CODE

There are different decoding methods for Convolutional codes which are Feedback decoding, sequential decoding and maximum likelihood decoding [2].

1. Threshold decoding **-** It is called majority logic decoding. It is successfully applied only specific classes of code. It applies to channel having mid to good SNR. It is far away from optimal because of its inferior bit error performance.
2. Sequential decoding **-** It is sub optimal. It has better performance than the previous method. Its advantage is decoding complexity is virtually independent from the length of the particular code. The drawback of sequential decoding is unpredictable decoding latency & variable decoding time. Also it requires large memory.
3. Viterbi decoding **-** It is optimal algorithm for decoding of Convolutional code. It is dominant technique for Convolutional codes. It has advantages like satisfactory bit error performance, low cost, fixed decoding time.

The viterbi algorithm proposed in 1967 is the most extensively decoding algorithm for Convolutional codes. It is powerful method for forward error correction. It has been widely deployed in much wireless communication system like IEEE 802.11a/g, Wi-Max, WCDMA and GSM to improve capacity of communication channel. The consumer demands for sophisticated portable wireless communication devices are high. So need for high speed viterbi decoder increasing.

II. BLOCK DIAGRAM

Here data at transmitter side is first encoded using adding redundancy bit which is called as convolution encoding. Encoded code is transmitted via Tx in wireless media and received at receiver side. At receiver side, data is decoded using viterbi algorithm. If any error is present in the code, that is corrected by viterbi decoder. Finally original data is available at receiver side. Block diagram of transmitter and receiver is shown in Fig No. 2.1 and Fig No. 2.2

TRANSMITTER

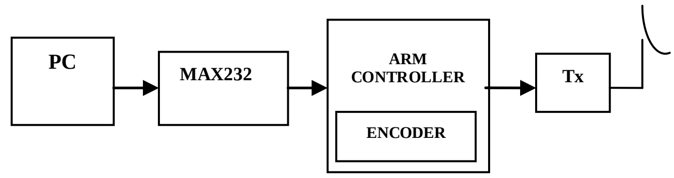


Fig. No. 2.1: Block diagram of transmitter side

RECEIVER

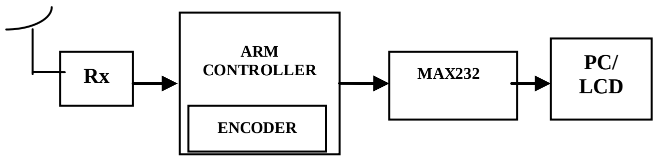


Fig. No. 2.2: Block diagram of receiver side

III. ERROR DETECTION AND CORRECTION TECHNIQUES

3.1 CONVOLUTIONAL CODES:

A] Code Parameters and the Structure of the Convolution Code [3]

The convolution codes are used for error correction. It is linear system. Binary convolution encoder can be represented by as a shift register.

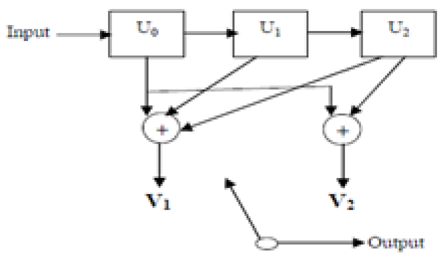


Fig. No. 3.1: Convolution Encoder

The output of the encoder is module-2 sum of the values in the certain register cell. Convolution codes are commonly specified by three parameters; (n, k, m), where ‘ n’ is the number of output bits, ‘ k’ is the number of input bits, and ‘ m’ is the number of shift register stages of the coder [5].

V1=U0 XOR U1 XOR U2 (1)

V2=U0 XOR U2 (2)

The constraint length L of the code represents the number of bits in the encoder memory that affect the generation of the n output bits and is defined as L = m k. The code rate ‘r’ of the code is a measure of the code efficiency and is defined by r = k/n.

B] Coding of code message –

Consider 3 bit sequence 110 it is given to encoder then it generate redundancy code sequence. Calculation is shown in Fig. No.3.1. In table 3.1 given below X1, X2 indicates present condition of shift register. V1, V2 indicates output of shift register which is encoded code.

Table 3.1 Coding of data bits

TIME INSTANT	INPUT	PRESENT CONDITION		OUTPUT	
		X1	X2	V1	V2
t=1	1	0	0	1	1
t=2	1	1	0	1	0
t=3	0	1	1	1	0
t=4	0	0	1	1	1

IV. IMPLEMENTTION OF VITERBI ALGORITHM:

Consider received sequence is 01 00 10 00 so trellis diagrams for that are shown in following Fig. no. 4.1
To reach output state there are different possible paths are present. As it is 8 bit received code sequence then input to convolution encoder is 4 bit. So there are 2^4=16 possible paths are present to reach output state i.e.a4, b4, c4, d4. The viterbi algorithm examines an entire received sequence of a given length. The decoder computes a metric for each path and makes a decision based on this metric. All paths are followed until two paths converge on one node. Hence calculate possible path for each state a4, b4, c4, d4 & running path metric for each state. It is shown in following table 4.1

Table 4.1 Path metric calculation

State	Possible Path	Running path Metric
a4	a0-a1-a2-a3-a4	2
	a0-a1-b2-c3-a4	5
	a0-b1-c2-a3-a4	3
	a0-b1-b2-c3-a4	5
b4	a0-a1-a2-a3-b4	4
	a0-b1-c2-a3-b4	5
	a0-b1-d2-c3-b4	5
	a0-a1-b2-c3-b4	3
c4	a0-a1-a2-b3-c4	3
	a0-b1-c2-b3-c4	4
	a0-b1-d2-d3-c4	3
	a0-a1-b2-d3-c4	6
d4	a0-a1-a2-b2-d4	3
	a0-b1-c2-b3-d4	4
	a0-b1-d2-d3-d4	3
	a0-a1-b2-d3-d4	6

Then the path with the lower metric is kept and the one with higher metric is discarded. The selected paths are called the survivors. For an N bit sequence, the total number of possible received sequences is 2^N only $2^{K(L-1)}$ of these are valid. The Viterbi algorithm applies the maximum likelihood principles to limit the comparison to $2^{K(L-1)}$ surviving paths instead of checking all paths. The most common metric used is the hamming distance metric. This is just the dot product between the received code word and the allowable codeword. These metrics are cumulative so that the path with the smallest largest total metric is the final winner. Here first path is selected which has minimum path metric

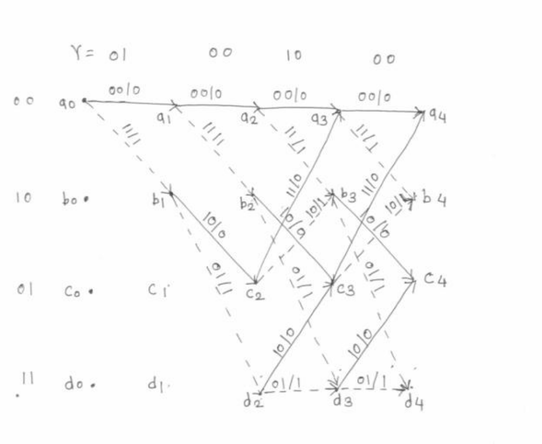
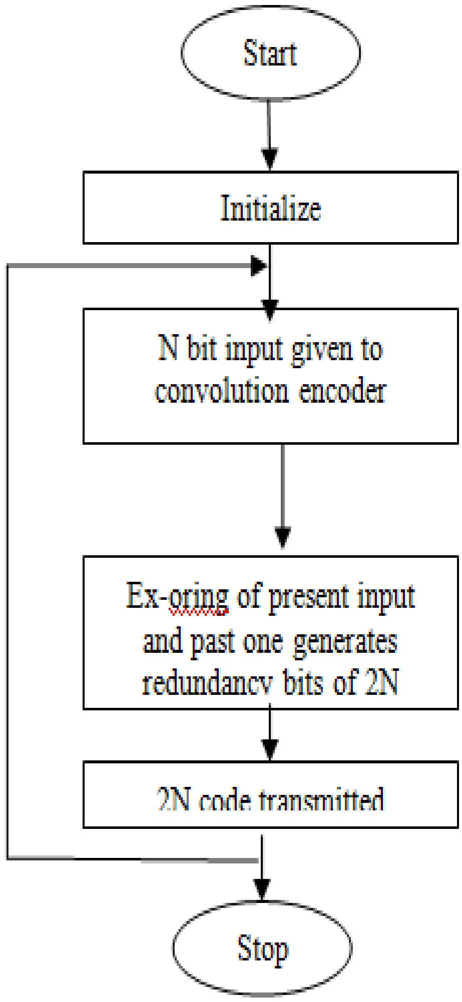


Fig. No 4.1 Trellis tree diagram

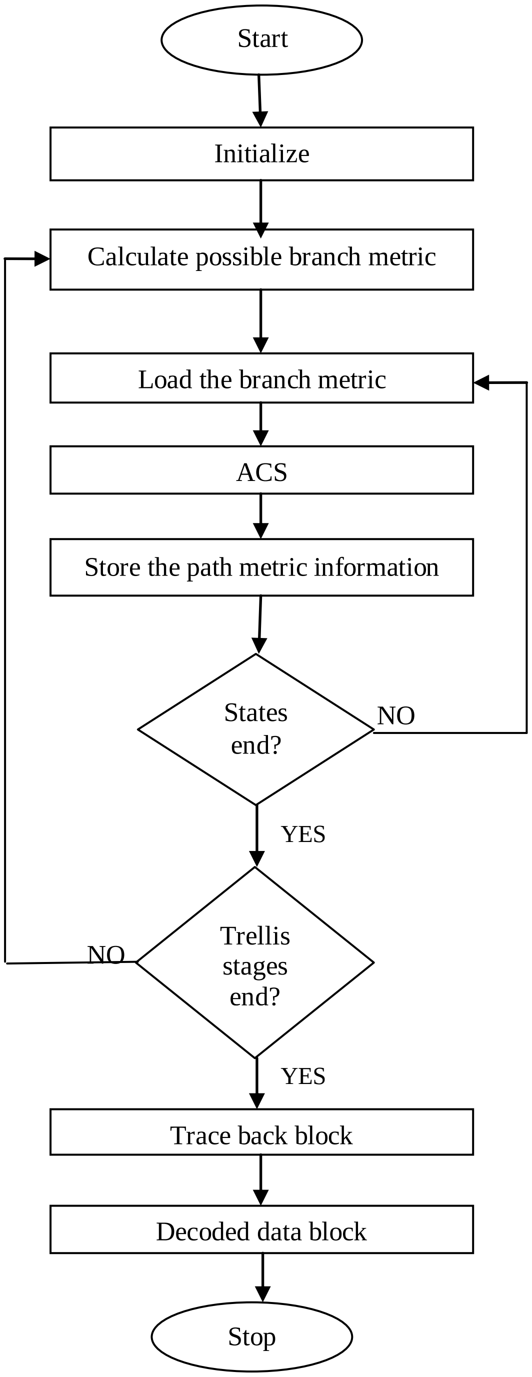
value then trace back path a0-a1-a2-a3-a4 to recover original value. Here decoded value is 00 00 00 00 means it indicates 2nd and 5th bit contain error. So this algorithm detects and corrects error.

V. SOFTWARE DESIGN

V.I FLOW CHART OF ENCODER OF VITERBI ALGORITHM:[6]



V.II FLOW CHART OF DECODER OF VITERBI ALGORITHM:



VI. CONCLUSION:

Viterbi decoder is one of the most important blocks in communication system. Viterbi algorithm allows safe data transmission via error correction and original message can recover accurately without any noise. In this work, error detection and correction techniques have been used which are essential for reliable communication over a noisy channel. The effect of errors occurring during transmission is reduced by adding redundancy to the data prior to transmission. Viterbi decoding is used for deep space communication, against impulsive noise with application to speech recognition, satellite communication and in many applications.[4]

Viterbi algorithm is mostly reliable for single bit error detection and correction. As number of error bits increases then efficiency of algorithm is decreases.

REFERENCES

[1] A. J. Viterbi, "Error Bounds for Convolutional Codes and an Asymptotically Optimum Decoding Algorithm," IEEE Trans. on Inf. Theory, vol. IT-13, pp.260-269, 1967
[2] ManjeetSingh, Ian J. Wassel "Comparison between Soft and Hard decision decoding using quaternary convolutional encoders and the decomposed CPM model", Laboratory for communications Engineering, Department of Engineering, University of Cambridge.
[3] Charon Langton, "Coding and decoding with conventional codes", www.complextoreal.com,July 1999
[4] A. J. Viterbi, "Convolutional codes and their performance in communication systems,"IEEE *Trans. Commun.*, vol. COM-19, pp. 751 - 772, Oct., 1971.
[5] Chip Fleming, "A tutorial on convolutional coding with Viterbi algorithm", 2003.
[6] H. Yang and X. Lang, "Design and implementation of high speed and area cefficient Viterbi decoder," IEEE, Proceedings of the 8th International Conference on Solid State and Integrating Circuit Technology, ICSICT'06, pp. 2108–2110, 2006