# Behavioral Design and Synthesis of 64 BIT ALU using Xilinx ISE

Rajib Chetia, Kaushik Chandra Deva Sarma, Gaurab Baruah

(Asst. Professor, CIT, Kokrajhar) (Asst. Professor, CIT, Kokrajhar) (M.Tech student .in ECT, Gauhati University)

*Abstract:* This paper presents the behavioral Design and synthesis of a 64 bit ALU. 64 bit ALU is basically a multiplexer that operates mainly 16 operations as per select line Bit-permutation. Flags are other important indicators used for specific purpose e.g. if Sign Flag is HIGH then the output of ALU must be a negative number. CLR can reset the output of ALU. *Keywords:* Flags, CLR, 64 Bit ALU, VHDL.

## I. Introduction

VHDL is used as the specification and synthesis language, but the process of transformation is substantially more automated. Specifically, the process of High-level simulation is maintained by the transformation from the level of description into hardware elements being automated. With the Synthesis route, the process of mapping into particular targeted circuit technologies is automated (e.g. Spartan 6E). The Synthesis process therefore both increases productivity (through automation) and reduces flexibility (by restricting the choice of technology.

### II. Behavioral Modeling

The Behavioral Style architecture contains concurrent statements with sections of sequential statements that describe the outputs of the circuit at a discrete moment in time given particular inputs. While similar language constructs are often found in Dataflow and Behavioral style architectures, only the latter explicitly exhibit the notions of time and control. This style describes the functions of the circuit at the algorithmic level. The highest level of abstraction is the behavioral level that describes a system in terms of what it does (or how it behaves) rather than in terms of its components and interconnection between them



Fig.1.1: Entity 64 Bit ALU

#### **3.1 Arithmetic Operations**

Carry Look Ahead Adder is a faster adder that overcomes the delay of Ripple Carry Adder. ALU can operate addition; subtraction etc. between Ain and Bin input bus.

## 3.2 Logic operations

All basic logic operations are included e.g. XOR, NAND, NOR, AND etc.

## 3.3 Flags Status

Flags are too much important in HDL Designing of ALU. All Flags like Sign, Overflow, Carry, Parity, Auxiliary Carry, and Zero. Flags actually allow us to determine the result of an operation more efficiently e.g. Overflow Flag shows occurrence of overflow condition during an operation.

## **3.4** Comparator

ALU compares the inputs Ain and Bin and results whether Ain>Bin, Ain=Bin or Ain<Bin.

## 3.5 Others

Enable, CLR are other parameters that are used to control the operations of ALU. CLR resets the output to logic 0. If Enable is set to logic 1 the ALU retains the value stored from previous clock cycle.



Fig. 1.2: RTL Schematic.

Table 1:						
SELECT	OPERATION	SELECT LINE	OPERATION			
LINE						
0000	Ain AND Bin	1000	Ain XNOR Bin			
0001	Ain OR Bin	1001	NOT (Ain NAND Bin)			
0010	Ain and (NOT Bin)	1010	NOT (Ain NOR Bin)			
0011	NOT Ain	1011	Carry Ripple Adder, Carry, Overflow			
0100	NOT Bin	1100	Carry Ripple Adder, Carry, Overflow			
0101	Ain NAND Bin	1101	64 Bit Adder			
0110	Ain NOR Bin	1110	64 Bit Subtractor			
0111	Ain XOR Bin	1111	Ain NOR (NOT Bin)			

## IV. Xilinx Simulation:

Simulation of 64 Bit ALU for the Behavioral model has been performed for 1000 nano-seconds (ns). Each Clock cycle has 100 ns rise time and 100 ns fall time. The simulation of 64 Bit ALU(if rising\_edge(CLK) and EN=0) generated from Testbench Waveform is given in figure 2.1 and 2.2 below.

Xilinx - ISE - C:\/	Mini Project\alu64\alu	u64.is	e - [Simulation]					
File Edit View	Project Source Proc	ess Tes	t Bench Simulatio	n Window Help				_ 6 2
🗋 🖻 🖥 🕼	5 X 6 6 X	12) (2)	0 0 0 0	( 🗶 🔎 🖻 🕅 🖪 🖻 🖻	🗅 🄑 😽 🛝	🗖 📝 🖉 🏟 🕽	(XXX 💡 3 O	
$\leftrightarrow$ $\mid$ $\equiv$ $n$	<u><u> </u></u>	% ⊕	1 1 th th	14030000	▶X 1000 💌 ns 💌			
Sources X Sources Behavi	Now:		0	200	400	600	000	9503)
- 🗑 alu64	1000 ns		0	200	400		800	-1
Cx x23 100e-44 Alv (alut Cy UUT Alv (alut Cy UUT Alv (alut Alv (alut Cy Cy C	of clk	0						
	off en	0						
	agb 🛛	1	Ū					و و و و و و و و و و و و و و و و و و و
	alb alb	0	U					
	aeb 😽	0						
	🖬 🚮 ain[63:0]	6	64'h0000 X	64'h5F27E6E87DB92DA0	64'hC83FA926AEDBA7E4	64'h91B3DF89690B8979	64'h1DB9E076BE9193F1	hEA31A7B 771C115
	🖬 🚮 bin[63:0]	6	64'h0000 X	64'h000BADC5556643FF	64'h5F27E6E87DB92DA0	64'hC83FA926AEDBA7E4	64'h91B3DF89690B8979	h1DB9E076BE9193
	carry_in	0						<b></b>
Processes X	🖬 🚮 select_l	4'h6		4'h0	4'h1 X	4'h5 X	4'h6	
Hierarchy of aluuu:	🖬 🚮 twos_com	6	64'hXXXXXX	64'hFFFC5B3FAADFFE60	64'h20C010110004501C	64'h80338900280B8161	64'h9DBBFFFFFF9B9BFA	FFB9E7 FFFFD19
🕀 🚺 aluuu - alu	🗉 🚮 outr[63:0]	6	(64'hUUUUUU)	64'h0003A4C0552001A0	64'hDF3FEFEEFFFBAFE4	64'h7FCC76FFD7F47E9F	64'h6244000000646406	00461800002E6
	zeros_counter	51	0	49	13	17	51	
	Carry_out	0	— <u>u</u> —					
	overflow	0						
	odd_parity	1	U					
	o zero	0	<u>U</u>					
	o ac	0	U					
	off sign	0	U					
۰ ( )	< - +	4 [] +	4					
Troc Sim H	Daluu yhd St De	esian Surr	mary aluuutt	w Simulation				3

Figure 2.1: Testbench Simulation.

Xilinx - ISE - C:\A	/ini Project\alu64\alu	64.is	e - [Simulation]					
File Edit View	Project Source Proce	ess Test	t Bench Simulatio	n Window Help				JU
🗋 🖻 🗑 🕼	8 X 6 6 X	10 (11	🖸 🏓 🔎 🕽	( 🗶 🔎 🖻 🕅 🖪 🗉 🛙	1 🗅 🎤 😽 🛝	💽 🗊 🖉 🕢 🏟 🕽	CRRX 💡 🛛 🔿	
	52 A % %	** •	1 1 th dr	11403 🖬 🦛 🕨	▶X 1000    ns			
Sources X								850.0
Sources Behavi	Now:			000	400	600	000	4000
- 😇 alu64	1000 ns		0	200	400	000	800	1000
⊟	öll cik	0				والمعادي المحددين ا		- <b>-</b>
au (au t	öll en	0						
E Aluuu (al	🎳 agb	1	<u>0</u>					وهد وهد ا
	oll alb	0	<u>0</u>					کک کی و
	aeb	0	<u>u</u>					
	🗖 🚮 ain[63:0]	6	64'h0000 X	64'h5F27E6E87DB92DA0	64'hC83FA926AEDBA7E4	64'h91B3DF89690B8979	64'h1DB9E076BE9193F1	hEA31A7B 371C115
	🖬 🚮 bin[63:0]	6	64'h0000 X	64'h000BADC5556643FF	64'h5F27E6E87DB92DA0	64'hC83FA926AEDBA7E4	64'h91B3DF89690B8979	xh1DB9E076BE9193
-C 2 69 Sr C L	carry_in	0						
Processes X	🖬 🚮 select_l	4'hE	4'h0 🔨	4'h9	4"hA	4'hD	4'hE	
Hierarchy of aluuu:	🖬 🚮 twos_com	6	64"hXXXXXXX	64'hFFFC5B3FAADFFE60	64'h20C010110004501C	64'hA60C774FE818CEA3	64'h73F9FF12AA79F588	338838ED4CD07
🕀 🚺 aluuu - alu	🖬 🚮 outr[63:0]	6	(64'hUUUUUU)	64'h0003A4C0552001A0	64'hDF3FEFEEFFFBAFE4	X 64'h59F388B017E7315D	64'h8C0600ED55860A78	CC77C742B32F8
	off zeros_counter	31	0	49	13	31	40	31
	oll carry_out	0	<u>u</u>					السلم المحل و
	overflow	0	<b>U</b>					السلم المحك ي
	odd_parity	1	<u>u</u>					
	o zero	0	<u>u</u>					
	oli ac	1	<b>u</b>					ورو ورو ال
	ol sign	1	<u>u</u>				i i i i i i i i i i i i i i i i i i i	
< +	۲ - F	4 🛛 F	4					•
Contract Proce Sim H	🛐 aluu.vhd 🛛 💆 De	sign Sum	imary 🔤 aluuu.t	ow Simulation				

Figure 2.2: Testbench Simulation

**V.** Synthesis and Implementation Report: Xilinx-ISE v9.1i has generated the Synthesis and Implementation report for the behavioral model of 64 Bit ALU and are given below:

Advanced HDL Synthesis Report Macro Statistics # Adders/Subtractors : 6 1-bit adder carry out : 1 2-bit adder carry out : 1 3-bit adder carry out : 1 3-bit adder carry out : 1 4-bit adder carry out : 1 5-bit adder carry out : 1 5-bit adder carry out : 1 6-bit adder carry out : 1 6-bit adder carry out : 1 6-bit adder carry out : 1	7 5 1
Macro Statistics # Adders/Subtractors : 6 1-bit adder carry out : 1 2-bit adder carry out : 1 3-bit adder carry out : 1 4-bit adder carry out : 1 5-bit adder carry out : 1 5-bit adder carry out : 1 6-bit adder carry out : 1 6-bit adder carry out : 1	5
# Adders/Subtractors: 61-bit adder carry out: 12-bit adder: 12-bit adder carry out: 13-bit adder: 33-bit adder carry out: 14-bit adder: 74-bit adder: 15-bit adder: 15-bit adder: 16-bit adder: 36-bit adder carry out: 1	5
<pre># Adders/Subtractors : 6 1-bit adder carry out : 1 2-bit adder carry out : 1 3-bit adder carry out : 1 3-bit adder carry out : 1 4-bit adder carry out : 1 4-bit adder carry out : 1 5-bit adder carry out : 1 6-bit adder carry out : 1 6-bit adder carry out : 1</pre>	5
1-bit adder carry out: 12-bit adder: 12-bit adder carry out: 13-bit adder: 33-bit adder carry out: 14-bit adder: 74-bit adder carry out: 15-bit adder: 15-bit adder carry out: 16-bit adder: 36-bit adder carry out: 1	5
2-bit adder : 1 2-bit adder carry out : 1 3-bit adder : 3 3-bit adder carry out : 1 4-bit adder carry out : 1 5-bit adder carry out : 1 5-bit adder carry out : 1 6-bit adder : 3: 6-bit adder carry out : 1	5
2-bit adder carry out : 1 3-bit adder : 3 3-bit adder carry out : 1 4-bit adder carry out : 1 5-bit adder carry out : 1 5-bit adder carry out : 1 6-bit adder carry out : 1 6-bit adder carry out : 1	5
3-bit adder : 3 3-bit adder carry out : 1 4-bit adder : 7 4-bit adder carry out : 1 5-bit adder carry out : 1 6-bit adder : 33 6-bit adder carry out : 1	5
3-bit adder carry out : 1 4-bit adder : 7 4-bit adder carry out : 1 5-bit adder carry out : 1 6-bit adder carry out : 1 6-bit adder carry out : 1	5
4-bit adder: 74-bit adder carry out: 15-bit adder: 15-bit adder carry out: 16-bit adder: 36-bit adder carry out: 1	5
4-bit adder carry out: 15-bit adder: 15-bit adder carry out: 16-bit adder: 36-bit adder carry out: 1	5
5-bit adder : 1: 5-bit adder carry out : 1 6-bit adder : 3: 6-bit adder carry out : 1	5
5-bit adder carry out : 1 6-bit adder : 3: 6-bit adder carry out : 1	1
6-bit adder : 3: 6-bit adder carry out : 1	1
6-bit adder carry out : 1	
64-bit adder : 1	
65-bit adder : 1	
65-bit adder carry in 1	
65-bit subtractor	( - I
••••••••••••••••••••••••••••••••••••••	-
# Registers : 7	78
Flip-Flops : 7	18
# Comparators : 3	2
64-bit comparator greater	
64-bit comparator less	1
# Multiplexers : 4	4
1-bit 16-to-1 multiplexer : 3	3
64-bit 16-to-1 multiplexer : 1	1
# Xors : 7	70
1-bit xor2 : 3	3
1-bit xor3 : 6	55
1-bit xor64 : 1	L
64-bit xor2 : 1	L
Timing Summary:	۲
Speed Grade: -4	
Speed Grade: -4	
Minimum period: 2.054ns (Maximum Frequency: 486.855MHz	:)
Minimum input arrival time before clock: 94.949ns	
Maximum output required time after clock: 10,535ns	
Maximum combinational nath delay: No nath found	
Principal Minimum Company (attrated where)	-1
Logic Utilization Used Available Utilization	
Number of Slices         857         960         897	1%
Number of Slice Flip Flops         65         1920         33	1 T
Number of 4 input LUTs         1521         1920         791	%
Number of bonded IOBs         279         108         2583	%
523.45 (STOR)	1% % %

## Figure 3: Design Utilization Summary.

## VI. Conclusion:

The 64 bit ALU is designed and synthesized using Xilinx ise v9.1i and targeted to Spartan device. The ALU is a major component of the CPU(Central Processing Unit). It performs arithmetic computation such as Addition, Subtraction, Comparator, Overflow and all basic logical operations (AND, OR, NOT, NOR, XOR, XNOR, NAND). We have verified the results obtained from Xilinx ISE Design Suit v9.1i with the theoretical results for all the operations that were performed and found that they match with the theoretical values.

#### **References:**

- Suchita Kamble1, Prof .N. N. Mhala "VHDL Implementation of 8-Bit ALU", IOSR Journal of Electronics and Communication Engineering (IOSRJECE) ISSN : 2278-2834 Volume 1, Issue 1 (May-June 2012)
- Engineering (IOSRJECE) ISSN : 2278-2834 Volume 1, Issue 1 (May-June 2012
  [2]. Geetanjali1 and Nishant Tripathi "VHDL Implementation of 32-Bit Arithmetic Logic Unit (Alu)" International Journal of Computer Science and Communication Engineering IJCSCE Special issue on "Emerging Trends in Engineering" ICETIE 2012
  [3]. D. Gajski and R. Khun, "Introduction: New VLSI Tools," IEEE Computer, Vol. 16, No. 12, pp. 11-14, Dec. 1983.
  [4]. D. L. Perry, "VHDL", Tata Mcgraw Hill Edition, 4th Edition, 2002.
  [5]. C. Maxfiled, "The Design Warriors Guide to FPGAs", Elsevier, 2004.
  [6]. J. Bhaskar, "VHDL Primer", Pearson Education, 3rd Edition, 2000.
  [7]. J. Bhaskar, "VHDL Synthesis Primer", Pearson Education, 1st Edition, 2002.