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Design and Analysis of 16 Bit Reversible ALU

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ABSTRACT : *Reversible or information-lossless circuits have applications in digital signal processing, communication, computer graphics and cryptography. Reversibility plays an important role when energy efficient computations are considered. Reversible logic is used to reduce the power dissipation that occurs in classical circuits by preventing the loss of information. This paper proposes a reversible design of a 16 bit ALU. This ALU consists of eight operations, three arithmetic and five logical operations. The arithmetic operations include addition, subtraction, multiplication and the logical operations include NAND, AND, OR, NOT and XOR. All the modules are being designed using the basic reversible gates. The power and delay analysis of the various sub modules is performed and a comparison with the traditional circuits is also carried out.*

Keywords - *Reversible logic circuits, Reversible logic gates, Reversible adder/subtractor, Reversible logic unit, Reversible ALU.*

I. INTRODUCTION

In modern VLSI system power dissipation is very high due to rapid switching of internal signals. The complexity of VLSI circuits increases with each year due to packing more and more logic elements into smaller volumes. Hence power dissipation has become the main area of concern in VLSI design. Reversible logic has its basics from thermodynamics of information processing. According to this, traditional irreversible circuits generate heat due to the loss of information during computation. In order to avoid this information loss the conventional circuits are modeled using reversible logic. Landauer [1961] showed that the circuits designed using irreversible elements dissipate heat due to the loss of information bits [1]. It is proved that the loss of one bit of information results in dissipation of KT*log2 joules of heat energy where K is the Boltzmann constant and T is the temperature at which the operation is performed. Benett [1973] showed that this heat dissipation due to information loss can be avoided if the circuit is designed using reversible logic gates [2]. A gate is considered to be reversible only if for each and every input there is a unique output assignment. Hence there is a one to one mapping between the input and output vectors. A reversible logic gate is an n –input, n- output device indicating that it has same number of inputs and outputs. A circuit that is built from reversible gates is known as reversible logic circuit.

In this paper, we design a 16 bit reversible ALU that can perform eight operations simultaneously. The eight operations include addition, subtraction, multiplication, division, AND, OR, NOT and XOR. All the modules are simulated in modelsim SE 6.5 and synthesised using Xilinx ISE 12.2.

II. REVERSIBLE GATES

Reversible logic is gaining importance in areas of CMOS design because of its low power dissipation. The traditional gates like AND, OR, XOR are all irreversible gates. Consider the case of traditional AND gate. It consists of two inputs and one output. As a result, one bit is lost each time a computation is carried out. According to the truth table shown in Fig.1, there are three inputs (1, 0), (0, 1) and (0, 0) that corresponds to an output zero. Hence it is not possible to determine a unique input that resulted in the output zero. In order to make a gate reversible additional input and output lines are added so that a one to one mapping exists between the input and output. This prevents the loss of information that is main cause of power dissipation in irreversible circuits. The input that is added to an m x n function to make it reversible is known as constant input (CI). All the outputs of a reversible circuit need not be used in the circuit. Those outputs that are not used in the circuit is called as garbage output (GO). The number of garbage output for a particular reversible gate is not fixed. The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Fig.1.Truth table of conventional AND gate

Fig.1 shows the truth table of conventional AND gate.In order to make this gate as reversible one input and two outputs are to be added so that it becomes a 3x3 reversible gate.

The main criteria while designing a reversible logic circuit is the minimization of the above mentioned parameters (CI, GO).

2.1 Basic Reversible Gates

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is shown in Fig.2. It is the only 2x2 reversible gate available and is commonly used for fan out purposes. Consider the input B as constant. When B is zero, the gate acts as a copying gate or a buffer where both the output lines contain the input A. When B is one, the complement of A is obtained at the output Q. The 3x3 reversible gates include Toffoli gate, Fredkin gate, New gate and Peres gate, all of which can be used to realize various Boolean functions. Fredkin gate is shown in Fig.3.The 4x4 reversible gates include TSG gate, MKG gate, HNG gate, PFAG gate etc. Fig.4 shows the TSG gate. Some of the 4x4 gates are designed for implementing some important combinational functions in addition to the basic functions. Most of the above mentioned gates can be used in the design of reversible adders.

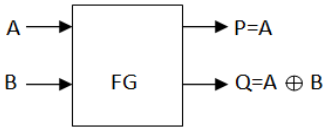

Fig.2. 2x2 Feynman gate

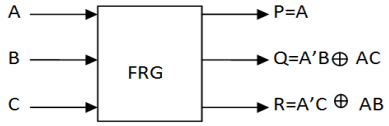

Fig.3. 3x3 Fredkin gate

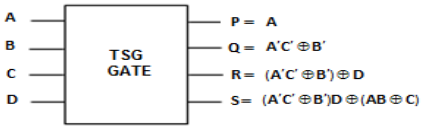

Fig.4.4x4 TSG gate

III. REVERSIBLE ALU DESIGN

3.1 Proposed Design

The Fig.5 shows the basic design of an ALU. For implementing a reversible ALU each of these basic components is implemented using reversible logic. The various sub modules in the design are adder/subtractor, multiplier and a logical unit. All the operations are performed simultaneously. On the basis of control signal, the required result is provided at the output.

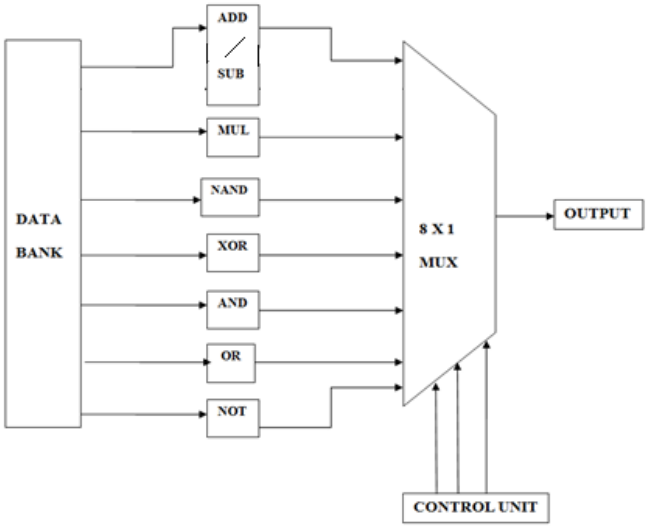

Fig.5. ALU design

3.2 16 Bit Adder/Subtractor Design

The binary full adder/subtractor handles each input along with a carry in /borrow in that is generated as carry out/borrow out from the addition of previous lower order bits. If two n bit binary numbers are to be added or subtracted then n binary full adder/subtractors should be cascaded. A parallel adder/subtractor is the interconnection of a number of full adder/subtractor and applying the inputs simultaneously. In this paper a 4 bit parallel adder/subtractor circuit is designed using a 4x4 reversible DKG gate. Fig.6 shows the reversible DKG gate. This gate can acts as an adder or subtractor depending on its control input 'A'. when 'A' is zero the gate behaves as a full adder and when 'A' is one the gate behaves as a subtractor. The block diagramm of a four bit reversible adder/subtractor using DKG gate is shown in Fig.7.

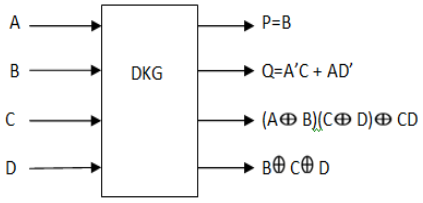

Fig.6. Reversible 4x4 DKG gate

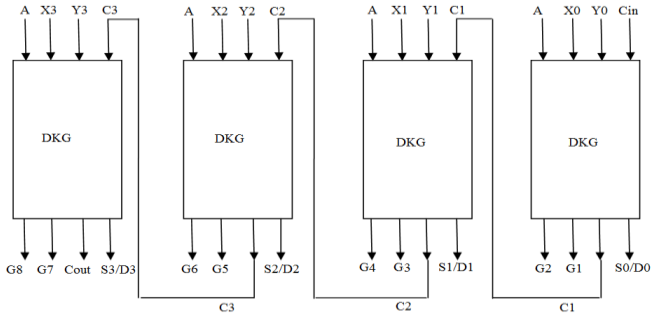

Fig.7. Reversible 4bit adder/subtractor

For implementing a 4bit reversible adder/subtractor, 4 DKG gates are required. Hence the total gate count for a 4bit adder/subtractor is 4 and that for a 16 bit adder/subtractor is 16. Here the carry in (Cin) is propagated from one gate to another gate. The module is designed using VHDL, simulated in modelsim and synthesized using xilinx12.2.

3.3 16 x 16 Multiplier Design

In this paper an n x n reversible multiplier is designed using TSG and Fredkin gates. The basic cell for such a multiplier is the full adder block. The TSG gate is shown in Fig.4. It is evident from the figure that the TSG gate can act as full adder when one of the inputs is assigned a constant value of zero [7]. In Fig.4 when c is assigned as zero the TSG gate acts as a full adder and the sum and carry output is obtained at S and R respectively. Fig.8 shows the TSG gate implemented as a full adder.

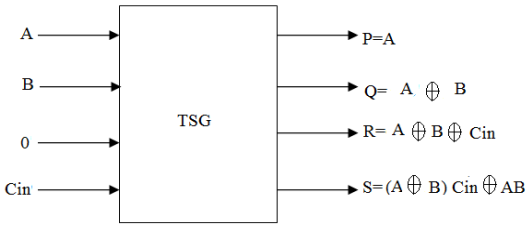

Fig.8. Reversible TSG gate as a full adder

Multiplication includes two basic steps. First step is the generation of partial products and the second one is the addition of the generated partial products. The partial products can be generated using Fredkin gate. When one of the input to the Fredkin gate is assigned a constant value of zero, then the Fredkin gate behaves like an AND gate and partial product can be generated as shown in Fig.10. The generated partial products can now be added using Parallel ripple carry adder that is designed by cascading the TSG gate. For a 4x4 multiplier, 16 Fredkin gates are required for generating the entire partial products. Three stages of reversible ripple carry adder using TSG gate is required for adding the above generated partial products and obtaining the final 8bit product.

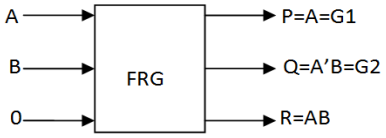

Fig.9 FRG gate used as AND gate.

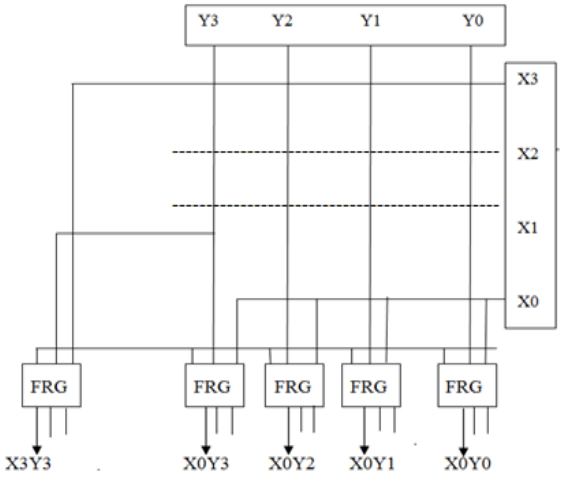

Fig 10. Generation of partial product

3.3.1 Multiplier Algorithm

The following algorithm can be used to design an 8x8 multiplier using 4x4 multiplier.

1. Let A and B be two 8 bit numbers that are to be multiplied.
2. Divide A into equal halves A1 and A0 such that A0 indicates the 4bit LSB and A1 indicates the 4bit MSB. Divide B also in the same way as B0 and BI.
3. Multiply A0 and B0 using reversible 4bit multiplier. This forms the first partial product PR1. Retain the

4bit LSB of PR1.

4. Now multiply A1 and B0. This forms the partial product PR2. Then multiply A0 and B1. This forms partial product PR3.

5. Add PR2, PR3 and the 4bit MSB of PR1 using reversible parallel adder designed from TSG gate. This forms the temporary result TR1. Retain the 4bit LSB of TR1.

6. Multiply A1 and B1 resulting in the partial product PR4. Now add PR4 and the remaining bits of TR1 (excluding the 4bit LSB) resulting in the temporary result TR2.

7. Now concatenate TR2 with the 4bit LSB of TR1 and PR1. This forms the final 16 bit product. The same can be applied for designing higher multipliers using lower multipliers.

Hence the total gate count for a 4x4 multiplier is 29 gates (16 Fredkin gates +13 TSG gates).

3.4 16 Bit Logical Unit

In this paper the logical block is designed using PFAG and Feynman gate. For designing a 1bit logical unit one PFAG and one Feynman gate is required. The truth table of PFAG is shown in Fig.12.

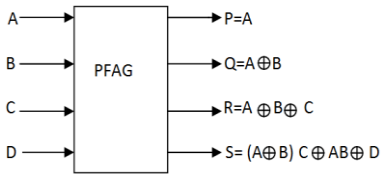

Fig.11 4x4 PFAG gate

Table.1. Truth table of PFAG

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	1	0
1	0	0	1	1	1	1	1
1	0	1	0	1	1	0	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	0	0
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

In this design the inputs C and D is taken as the select lines or control lines.

When CD=00 the PFAG block acts as an AND gate and the output of the AND operation between A and B is obtained at S. When CD=01 the NAND operation between A and B is performed and the output is obtained at S. When CD=10 the OR operation between A and B is performed and obtained at S. The XNOR operation between A and B is obtained at R. When CD=11 the NOT operation of A is carried out and obtained at P1. The XOR operation of A and B is obtained at Q irrespective of the value of C and D. The block diagram of PFAG gate is shown in Fig.11. The design of 1bit logical unit is shown in Fig.12.

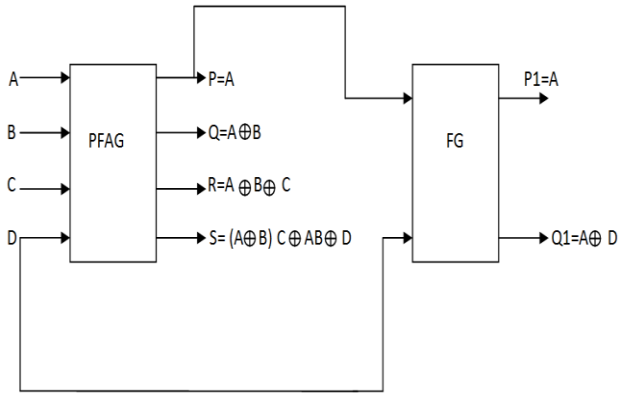

Fig.12. Design of one bit logical unit

The above design requires a total of 32 reversible gates (16 PFAG + 16 FG) for implementing a 16bit reversible logical unit that can perform AND ,OR, NOT,XOR,NAND and NOR.

IV. SIMULATION RESULTS

All the blocks are modelled using VHDL. The functional verification of the codes is analysed using modelsim 6.5 and synthesised using Xilinx ISE 12.2.

4.1 16 Bit Reversible Adder/Subtractor

Fig.13 shows the output of 16 bit reversible adder/subtractor. The inputs to this module are the 16bit data 'A', 'B' and a control signal 'A/S'. When the control input is '0', the addition operation is performed and when the control input is '1' subtraction operation in carried out. 'Cin' indicates the carry in, Cout indicates the carry out or borrow out obtained from the circuit.

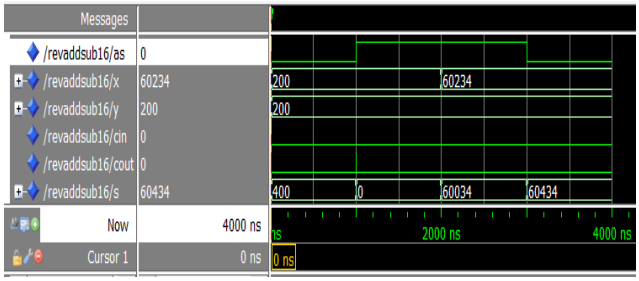

Fig.13. Reversible 16bit adder/subtractor

4.2 16 Bit Reversible Logical Unit

Fig.14 shows the output of reversible 16 bit logical unit. Here A and B indicates the 16bit data. C is a two bit input data that acts as the control signal. Depending on this value the required output results are obtained. AD denotes the AND output, XR denotes the XOR operation, O denotes the OR output and NT denotes the NOT operation.

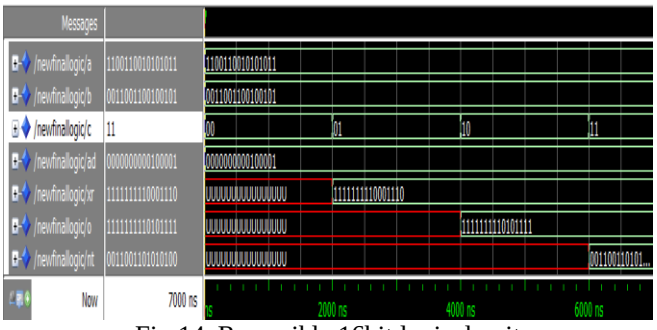

Fig.14. Reversible 16bit logical unit

4.3 16 x 16 Multiplier Unit

Fig.15 shows the output of 16 x 16 reversible multiplier. X and Y indicate the 16 bit input data and PRD indicates the 32bit output data. Here PR1, PR2, PR3 and PR4 are the various partial products that are generated in the multiplication process. All the above mentioned sub modules are integrated together to form a 16 bit ALU.

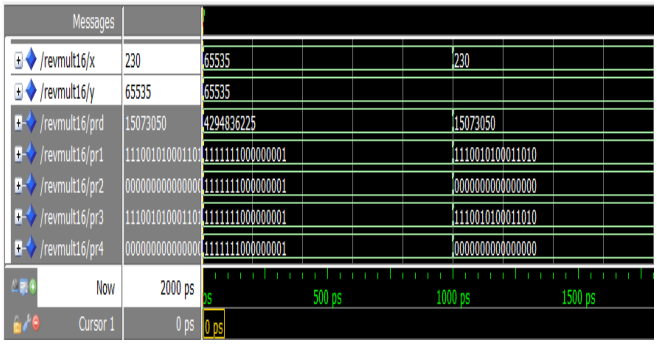

Fig.15. Reversible 16 x 16 multiplier

V. SYNTHESIS REPORTS

The delay and power analysis reports of the various submodules are also carried out. The power analysis reports are carried out using synopsys design compiler. The comparison of reversible and conventional submodules in terms of power and delay is evaluated.

5.1 Reversible Adder/ Subtractor

5.1.1 delay analysis

Table 2 shows the delay analysis of reversible and conventional 4bit adder and subtractor. It can be deciphered from the figure that reversible adder and subtractor shows 14% reduction in delay in comparison with conventional adder and subtractor.

Table 2. Delay analysis of 4bit adder and subtractor

	Ripple carry adder	Reversible adder	Basic subtractor	Reversible subtractor
Delay(ns)	9	7.88	9.2	7.94

5.1.2 Power analysis

Table 3 shows the power analysis of reversible and conventional adder and subtractor. Reversible adder and subtractor shows 25% power reduction in comparison with the conventional adder and subtractor.

Table 3. Power analysis of 4bit adder and subtractor

	Ripple carry adder	Reversible adder	Basic subtractor	Reversible subtractor
Power (uW)	15.2617	11.3997	16.5745	12.3500

5.2 Reversible Multiplier

5.2.1 delay analysis

Table 4 shows the delay analysis of reversible and conventional multipliers. The reversible multipliers show a better delay in comparison with the traditional multipliers.

Table 4. Delay analysis of reversible and conventional multipliers

	4x4con. multiplier	4x4rev. multiplier	8x8con. multiplier	8x8rev. multiplier	16x16con. multiplier	16x16rev. multiplier
Delay (ns)	12.760	12.644	21.524	21.440	43.198	41.178

5.2.2 Power analysis

Table 5 shows the power analysis of reversible and conventional multipliers. The reversible and conventional multipliers show 23% power reduction in comparison with the conventional multipliers.

Table 5. Power analysis of reversible and conventional multipliers

	4x4con. multiplier	4x4rev. multiplier	8x8con. multiplier	8x8rev. multiplier	16x16con. multiplier	16x16rev. multiplier
Power	53.256uW	36.376uW	393.801uW	299.868uW	2.10mW	1.6mW

V1. CONCLUSION

The 16 bit reversible ALU is designed by integrating various sub modules that includes adder/subtractor, multiplier and logical unit. The logical unit performs AND, OR, NOT, XOR, NAND. The performance evaluation of the various submodules are carried out using synopsys tools and it was found that the circuits designed using reversible logic showed a reduced dealy and power. As a future work a reversible divider can also be designed and included into this ALU.

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