HDL Design for Exa Hertz Clock based $2^{e^{23}}$-1 Exa Bits Per Second (Ebps) PRBS Design for Ultra High Speed Applications/Products

P.N.V.M Sastry $^1$, Dr.D.N.Rao $^2$, Dr.S.Vathsal $^3$

$^1$(Professor &Dean-Real Time It Eda Software Mnc Industry & R&D Cell & Ece J.B.R.E.C, India)
$^2$(Former Principal –J.B.R.E.C & Professor & Head -Ece ,Dean R&D, J.B.I.E.T, India)
$^3$(Former Dean R&D – J.B.I.E.T & Professor – Ece, I.A.R.E, India)

Abstract: The Design is mainly Intended for HDL Design for Exa Hertz Clock based $2^{e^{23}}$-1 Exa Bits Per Second (Ebps) PRBS Design for Ultra High Speed Applications/Products the estimation of HIGH Speed in terms of Ebps(Exa Bits Per Second) Data Rate for $2^{e^{23}}$.1 Tapped PRBS Design Pattern Sequence. The Exa Bits Per Second Data Baud rate Speed estimated by Synchronization with Exa Hertz Clock (2$^{30}$ Clock Cycle Periodic time for 1 Exa Hertz Clock frequency ) The Exa Hertz E.B.P.S $2^{e^{23}}$-1PRBS is Designed by using LFSR Linear Feed Back Shift Register & XOR Gate with Specific Tapping Points(18 and 23) as per CCITT ITU Standards and this design block Purely Synchronized with Exa Hertz Clock. RTL Design Architecture Implemented by using VHDL &/Verilog HDL, Programming & Debugging Done by using Spartan III FPGA Kit. Transmission done through this carrier frequency. Propagation Carrier Done either Serially/Parallel lines I/O in FPGA.

Keywords: CCITT – Consulting Committee for International Telegraph & Telecom , ITU – International Telecom Unit, LFSR-Linear Feedback Shift Register, PRBS-Pseudo Random Binary Sequence. RTL- Register Transfer Level , VHDL- Very High Speed Integrated Circuit Hardware Description Language.

1. Introduction

In Modern Hi-tech Communication Engineering-world, High Speed based Portable Communication System Hardware & Software Products Came to the market, speed is an important factor and is in terms of Giga bits per second for all Hi-tech Real time Smart Computing Portable wireless Communication System Software products like Cloud Computing, wireless Internet Data Packets Transceivers Computing, Tablets, Pocket Mobile Multimedia Systems, Note Book Computers, Wireless Routers, NOCs, Network Cards /Racks, WiFi, GiFi, Wimax, GPS, G SM, QCDMA Transceivers. For that purpose I Designed Exa Bits Per Second, Exa Bits Per Second High Speed PRBS is Pseudo Random Binary Sequence Frequency Generators, Generate & Received Random Frequency Data in the form of Random frequency numbers of different speed w.r.t specific data tapping sequence points for both signal & carrier wave generation. PRBS Generators, Receivers, Transceivers Designed for Hi-Fi Wireless Internet Data Packets Computing and Cloud Computing etc. Transmission, Reception of Data is in the RANDOM Sense, This PRBS Generator, Receiver is Designed for Identification property of Different Tapped PRBS Sequences like 7,10,15,23,31 at a Clock carrier-frequency speed of Tbps(Exa Bits Per Second). The Length of PRBS sequence is $2^{k}-1$. $2^{k}-1$ times repeated the sequences, this is mainly suit for multiple users to transmit and received data in accurate time for very long distance communications like GPS Data Acquisition, G.S.M-Communication Systems, WiFi, GiFi, LTE, Wireless O.F.D.M.A,C.D.M.A, Q.C.D.M.A Computing, wireless internet computing, cloud computing etc because of Ultra High speed Communication Rate in terms G.b.p.s, T.b.p.s, P.b.p.s ,Ebps. All these PRBS LFSR Sequences are designed by tapping different points according to ITU O.150, O.151,O.152 Standards. This PRBS Design Consists of Multiplexer, PRBS Registers of different tapped sequence points, Clock Frequency Generators of Ebps Speed. The Advantages of these PRBS Generators having In Built Checkers, Bit Error Rate Detection & Correction by using PRBS Checkers, these are simply Linear Polynomial Checkers & CRC.

1.1 Fibonacci (Many To One ) Realization of Lfsr

![Fig(1). Fibonacci (many-to-one) realization of LFSR with minimum number of taps and XOR gate in its feedback](image-url)
II. $2^{23} - 1$ E.B.P.S - PRBS DESIGN

![Diagram](image)

Fig(2). Exa Hertz Clock (E.b.p.s) $2^{23} - 1$ PRBS Design

1.2 Description:

The Exa Hertz Clock (E.b.p.s) $2^{23} - 1$ P.R.B.S A.S.I.C Design Consists of 32 Bit L.F.S.R and Tapping Points 18 and 23 are Feed back to the Input of XOR Gate and the Output of XOR gate is connected to the input of 32 Bit L.F.S.R(Linear Feedback Shift Register). the 32 Bit L.F.S.R Designed by using 32 1 Bit D Type Flip Flop Delay Elements, shift the Data Bits through 32 Bit L.F.S.R, the maximum length of the Seed Word Pattern sequences generated is $2^{23} - 1$. the P.R.B.S is Purely Synchronized with Exa Hertz Clock Cycle and the Baud Rate speed Generated by the Exa Hertz clock is E.b.p.s (Exa Bits Per Second) Rate. the Exa Hertz Clock Oscillator is Designed by using 50 Bit Exa Hertz Counter, that generates $2^{50}$ Clock Cycles for one Clock Cycle Period (Half of $2^{50}$ for One Exa Hertz Positive Clock Cycle Period and other of half of $2^{50}$ for One Exa Hertz negative Clock Cycle. The Significance of Tapping is for Generation of High Speed Carrier wave Frequencies in terms of Multiple Giga Hertz at Exa Hertz Clock Frequency and the speed of Clock is Exa Bits Per Second and The Data transmission speed is in terms Exa Bits Per Second, it is purely synchronized with Exa Hertz Clock. Design Implementation Done through SPARTAN III FPGA and Software Coding Development Done by Verilog HDL and VHDL and Test Benches Code also written in same Verilog HDL and VHDL. Software Process flow Implementation Done by Xilinx ISE Process Design and Implementation.


![Diagram](image)

Fig(3). VLSI Design Flow Chart $2^{23} - 1$ E.b.p.s P.R.B.S A.S.I.C I.P CORE

1.3 Description.

IV. P.R.B. S Tapping Frequency Table

<table>
<thead>
<tr>
<th>PRBS TYPE</th>
<th>STANDARD</th>
<th>SUGGESTED DATA RATE (Kilo Bits Per Second)</th>
<th>FEED BACK TAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>2(^{7})-1</td>
<td>ITU-T O.150</td>
<td>14.4</td>
<td>7.6</td>
</tr>
<tr>
<td>2(^{10})-1</td>
<td>ITU-T O.150</td>
<td>64</td>
<td>10.3</td>
</tr>
<tr>
<td>2(^{15})-1</td>
<td>ITU-T O.150</td>
<td>1544, 2048, 6312, 8448, 32064, 44736</td>
<td>14.15</td>
</tr>
<tr>
<td>2(^{23})-1</td>
<td>ITU-T O.150</td>
<td>34368, 44736, 139264</td>
<td>18.23</td>
</tr>
<tr>
<td>2(^{28})-1</td>
<td>ITU-T O.150</td>
<td>28, 31</td>
<td></td>
</tr>
<tr>
<td>2(^{31})-1</td>
<td>ITU-T O.150/151/152</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2(^{48})-1</td>
<td>ITU-T O.150/151/152</td>
<td>48.42</td>
<td></td>
</tr>
<tr>
<td>2(^{63})-1</td>
<td>ITU-T O.150/151/152/153</td>
<td>52.47</td>
<td></td>
</tr>
</tbody>
</table>

Table(1). PRBS Tapping Frequency Design


5.1 2e23-1 Exa Hertz Clock (Ebps) PRBS DESIGN RTL BLOCK

![Fig(4). R.T.L Design Block 2e23-1 Exa Hertz Clock (E.b.p.s) P.R.B.S A.S.I.C](image)

5.2 RTL Schematic 2e23-1 Exa Hertz Clock (E.b.p.s) P.R.B.S A.S.I.C

![Fig(5). R.T.L Schematic Block 2e23-1 Exa Hertz Clock (E.b.p.s) P.R.B.S A.S.I.C](image)

5.3 F.P.G.A PLACED DESIGN REPORT -2e23-1 Exa Hertz Clock P.R.B.S A.S.I.C

![Fig(6). F.P.G.A PLACED DESIGN - 2e23-1 Exa Hertz Clock P.R.B.S](image)
5.4 F.P.G. A Routed Design $2e^{23}$-1 E.b.p.s P.R.B.S A.S.I.C DESIGN ROUTED Report

VI. Simulation Wave Form Results

VII. Conclusion

$2e^{23}$-1 Exa Hertz Clock Based (Ebps Baud Rate Cycle Speed) PRBS A.S.I.C Design for High Speed Random Carrier Frequency Generator for Ultra High Speed Wireless Communication Engineering Products

HDL Design for Exa Hertz Clock based 2e^{23} -1 Exa Bits Per Second (Eb/s) PRBS Design for Ultra

Workshops etc. Recently Invited me as a Reviewer of IEEE TENCON-16, Singapore.

Dr. D.N Rao B.Tech, M.E, Ph.D, earlier principal of JBREC, Hyderabad. And Professor & HOD JBIET. His carrier spans nearly three decades in the field of teaching, administration, R&D, and other diversified in-depth experience in academics and administration. He has actively involved in organizing various conferences and workshops. He has published over 11 international journal papers out of his research work. He presented more than 15 research papers at various national and international conferences. He is Currently approved reviewer of IASTED International journals and conferences from the year 2006. He is also guiding the projects of PG/Ph.D students of various universities.

Dr. Vathsal Currently working as a Professor & Dean- R&D & EEE, JBIET. He Obtained PhD from I.I.S.C, Bangalore, also Did Post Doctoral Research in DFVLR, Germany and NASA Goddard Space Flight Centre, USA, and also he worked with keen Designations Scientist E,F,G from Reputed Govt R&D Industry Organizations over past years and closely worked with Dr. A.P. J Abdul Kalam. He Published lot of various national, international journals & conferences. He guiding 5 PhD Students from Various universities. He Got Prestigious awarded as a Noble Son of India.