

Circuit Nanotechnology: QCA Adder Gate Layout Designs

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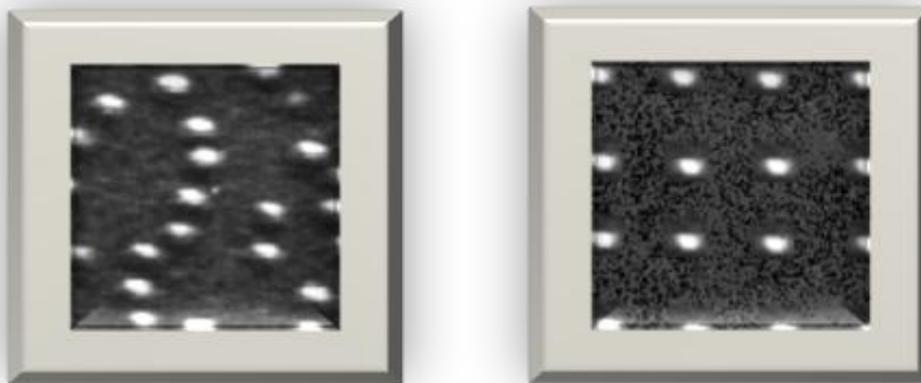
Abstract : Quantum-dot Cellular Automata (QCA) based circuit designs have been explored since its concept development in early 1980's. Although there are lot of implementation barriers for the development of this nanotechnology to work smoothly at room temperature but the simulated circuit implementations have attracted a large number of researchers towards this new field. The success of metal dot implementation even at very low temperatures has paved a way for exploring new possibilities in computing paradigm. An ample of circuit layouts have been proposed for the design of EX-OR gate, a vital element for arithmetic processes. We have analyzed some reported layouts in terms of their simulation accuracy, latency, cell count and noise performance to propose few single layer robust circuits for their efficient implementation.

Keywords: QCA Cell, Electrostatic noise, Simulator, Tunneling, Majority gate, Lattice structure.

I. INTRODUCTION

In the quest for finding alternatives of the classical models of continuity with discrete models based on quantum concepts various ideas were explored since the development of quantum mechanics. Quantum computing (QC), cellular automata (CA) and quantum-dot cellular automata (QCA) are all explorations based on discrete system. The system of device design based on electron positioning gave birth to concept of quantum-dot in early eighties. A quantum-dot thus can be defined as a nano scale vessel in which an electron can be trapped. Dot as such can be termed as a potential well or potential ring in which a sufficiently low energy/ low temperature electron can be trapped. There are several ways of implementing quantum-dots but the tested and commonly explored is Aluminum metal-dots developed with the help of electron lithography.

At Notre Dame University the researchers proposed the logical unit of QCA as QCA-cell composed of four or five quantum-dots. As the dots have the ability of confining an electron in 3-dimensional space, it is suggested to prove backbone in future micro or what will be called as Nano-electronics or Nano-optoelectronics. This can lead to application development in tunable-lasers, photo-detectors, neuro-quantum structures, sensors, single electron devices and quantum cellular automata [1, 2, 3, 4, 5]. The dots produced with the help of electron beam lithography are not having a similar shape but varied shapes depending on the process and application.



Dots Produced

Dots Desired

Figure (1)

There are various processes of producing these devices and one of big challenges to achieve the objective is the precise location of quantum dots at the desired locations. Self organization is one of these processes and occurs when molecules of one crystal structure is deposited on the top of another. The lattice structure difference results in high stresses at the point of contact as such the material tends to clamp up at the point of contact in a manner of depositing oil on water.

Although this process can produce dots of incredibly small size but one big problem is that the dots are not located at desired places. Figure (1) shows the uneven placement of produced dots with a projected image of required dot placements for the purpose.

1.1 Quantum-Dot Cell

A cell is a device used to store and transmit data using electrons and the Columbic interactions. The electrons change orientations from 0 to 1 or vice-versa by changing positions through electron tunneling. A four dot quantum cell with two excess electrons is shown in Figure (2) representing two binary states of 0 (zero) and 1 (one) and the arrangement will always place the electrons in the opposite corner or antipodal positions due to their repulsive force on each other. C. S. Lent and W. Porod at Notre Dame University proposed a wireless two state quantum device cell of five dots as shown in Figure (3). The modal similar to four dot cell modal and likewise yields two states of equal energy in the cell.

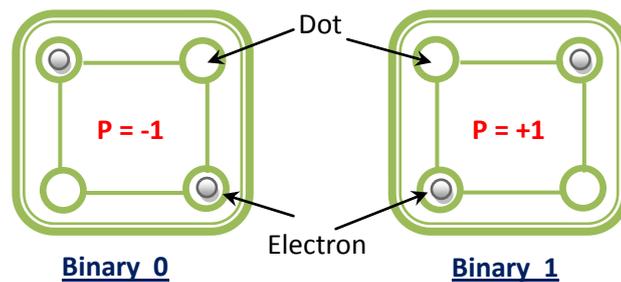


Figure (2)

1.2 Cell Working

The electrons in the cell always have the antipodal sites in both states of logic one (1) and logic zero (0) but the alignments are opposite as shown in figure (2) and figure (3). If two cells are brought close to each other they get aligned in the same direction due to inter columbic interaction as shown in Figure (4). The cells assume the order of lower energy in the system. In other words if a cell among two adjacent cells is brought to a

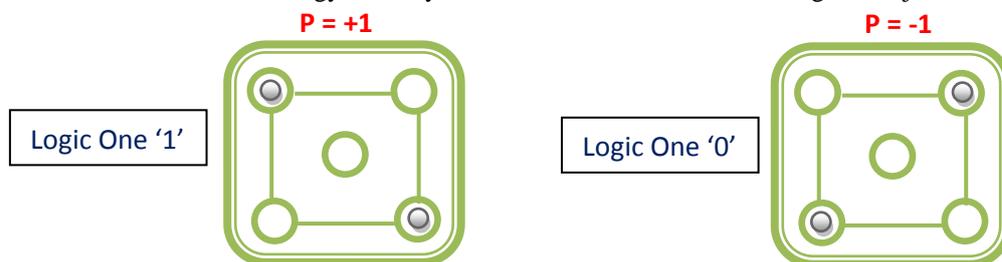


Figure (3)

state of '0' or '1' the adjacent cells will also get into same state. The carriage of state from one cell to its adjacent cell is said to have transmitted data and if number of cells are placed adjacent to each other the data will travel from one end to other. Although no current flows but the conduction has taken place. This sort of conduction is the basic principle behind the working of quantum-dot cell devices. The shift of electron from one dot to other is facilitated with the help of tunnel capacitor junction between the dots. Known as Dolan bridge technique [6] this

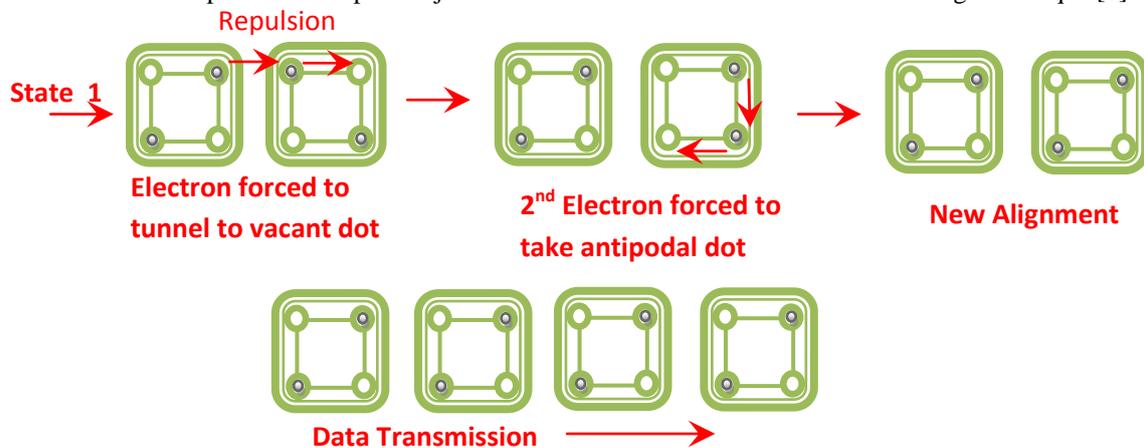


Figure (4)

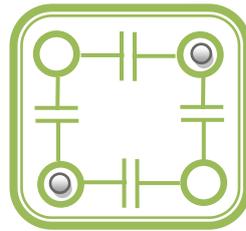


Figure (5)

physically embeds a capacitor junction between the dots in a quantum cell. As the repulsive force is encountered by an electron from the adjacent electron it tunnels through Dolan bridge junction to the adjacent vacant dot. The Dolan bridge junction between the dots in a quantum cell is demonstrated in Figure (5) above.

II. DEVICE SURVEY AND ANALYSIS

The logical device design with the help of quantum cells in the laboratory is not possible everywhere as the technology is still in its initial development stage and the research work is continue for the development of such cells at room temperature. However on the basis of the basic properties of the quantum cells developed at Notre Dame University different algorithms have been designed to explore the possibilities of the devices with the help of software simulations. QCA Designer [7] is the mostly used software for simulations of QCA layout assemblies. While most of the researchers explore the possibility of circuit layouts with help of QCA Designer the work continues with various options like molecular and solid state devices to have a stable technology operating at room temperature [8] for mass application in the future equipment. We have also studied and analyzed different logical device layouts with the help of QCA Designer software tool to arrive at some definite robust conclusions. As discussed above the quantum-dot cells arranged in a line produce a sort of conduction, this assembly of cells is termed as wire. A wire simulation is carried out by arranging a number of cells in a line and making the one end as input with respect to the other. The assembly and the simulation result are given in Figure (6-a). Second important thing is to draw several output lines from a single input, this is termed as Fan-out. A fan-out is extension of the wire layout design demonstrated above and the only difference is to watch the similar waveform appearing at different output lines. The circuit layout and the simulation waveforms are presented in Figure (6-b). The logic NOT operation in QCA is performed in different ways and two ways to achieve this objective have been simulated by us for the demonstration. Circuits with two types of NOT possibilities are given in Figure (6-c).

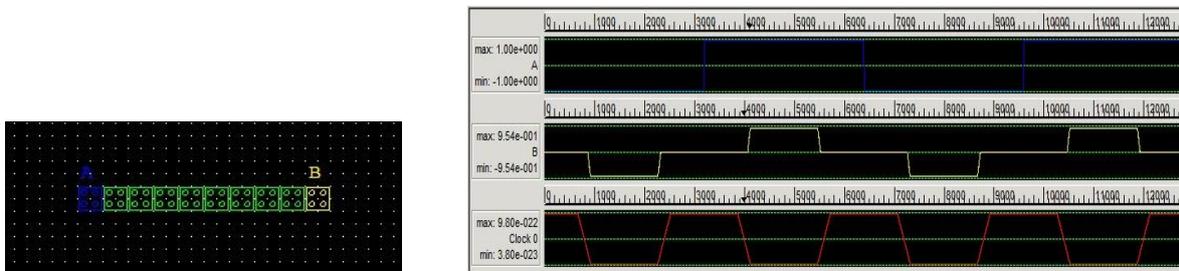


Figure (6-a)

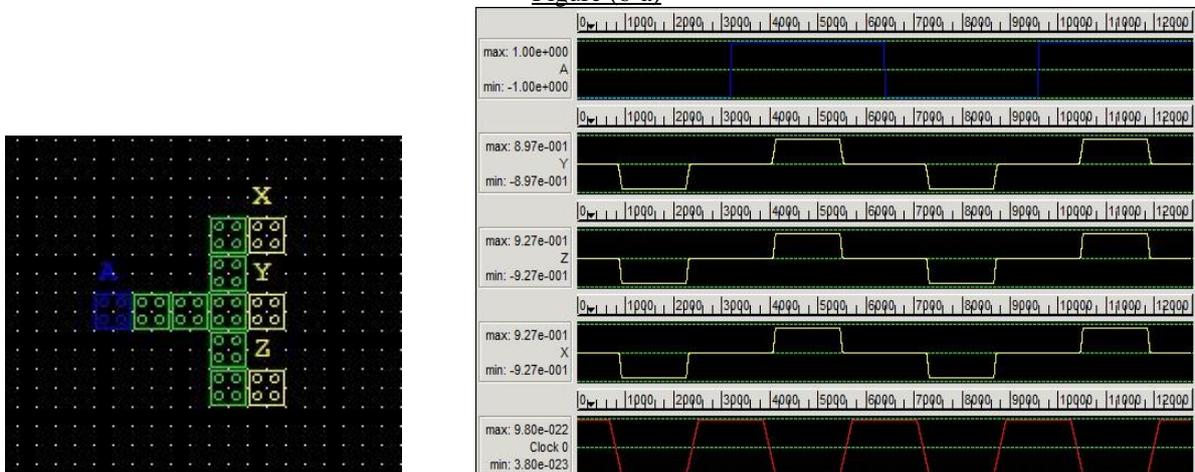


Figure (6-b)

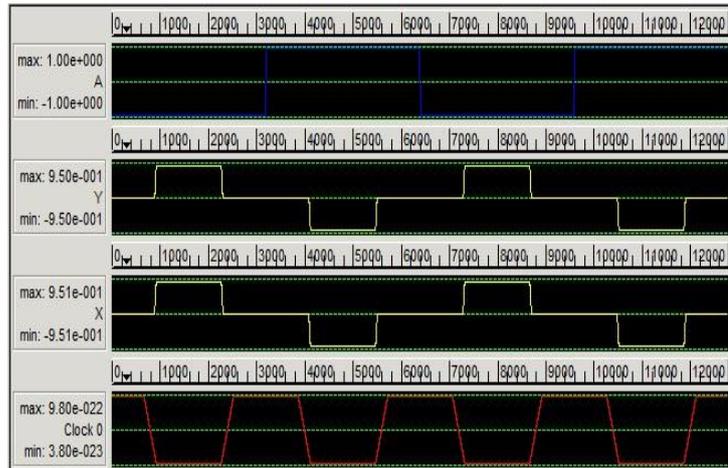
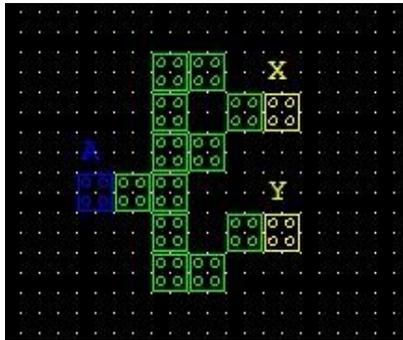
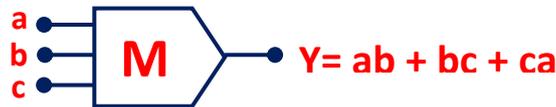


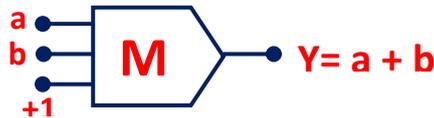
Figure (6-c)

Fundamental gate for the QCA exploration has been identified as the majority gate. It has three inputs and an output and its output is high when at least two of its inputs are high. The symbol and logic expression for the gate is given below:



This gate is implemented by few quantum cells and has been demonstrated in the Notre Dame laboratory. The gate has a versatile property of acting as AND and OR gate with simply fixing one of its inputs. Let us assume the c input of the above to be at logic one i.e. $c = +1$ the Boolean expression for the above gate becomes

$$\begin{aligned}
 & Y = ab + a + b \\
 \text{Or} & \quad Y = a(b+1) + b && \text{since } b+1 = 1 \\
 \text{Therefore} & \quad Y = a + b && \text{(OR gate)}
 \end{aligned}$$

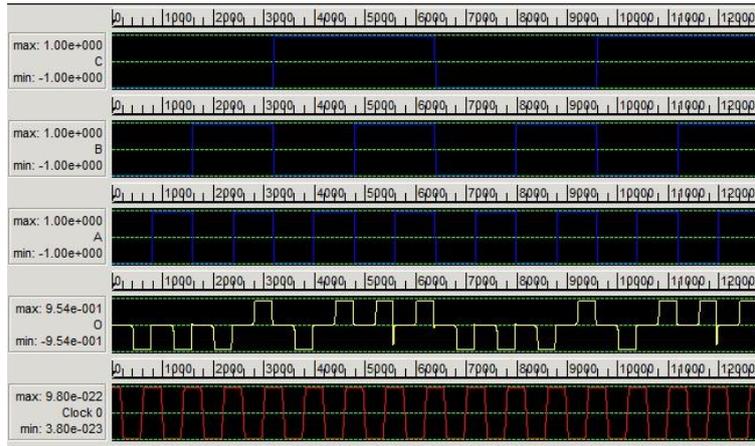
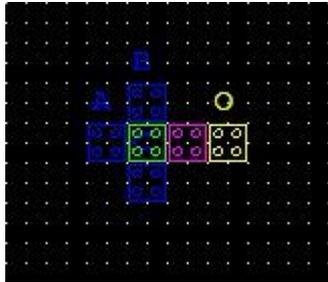


In the similar way if the c input of the majority gate is fixed to logic '0' zero i. e. $c = -1$ the Boolean expression for the gate becomes

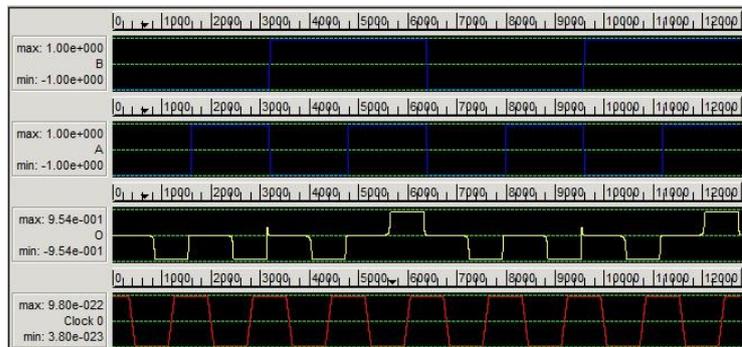
$$\begin{aligned}
 & Y = ab + 0 + 0 \\
 \text{Or} & \quad Y = ab && \text{(AND gate)}
 \end{aligned}$$



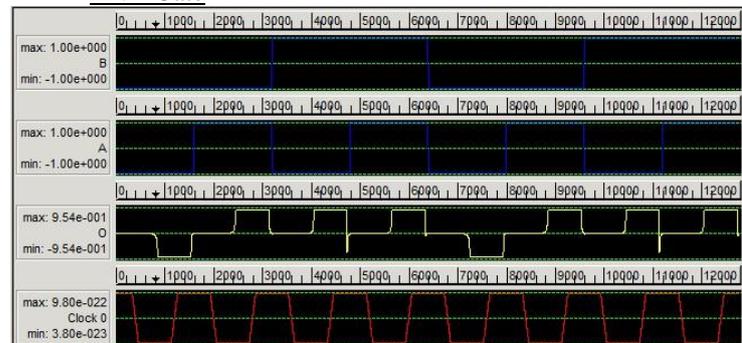
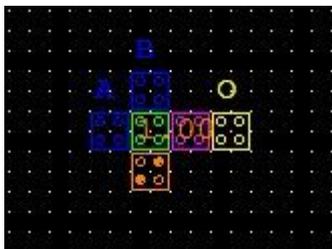
Hence having NOT and the Majority gate to design OR and AND gates one has ample liberty to implement any kind of Boolean expression used for circuit design in digital electronics. Cell layout and simulation result for AND, OR and Majority gates has been reported by maximum researchers on five cell assembly. We have observed some noise distortion in the output as such an addition of one more cell at output stage was observed to produce robust results. The layouts along with simulation wave forms are presented in Figure (7) below:



Majority Gate



AND Gate



OR Gate

Figure (7)

Implementation of other logic gates like NAND and NOR can be simply designed by putting a NOT gate at the output of AND and OR gates respectively. The symbolic representation along with Boolean expression for these gates is given in Table (1). The main problem in the design arises when we start simulations for the Exclusive-OR and Exclusive-NOR gates. The gates as we know are designed with the assembly of few gates, the layout imbalance and the clocking zone extensions produce interference in the produced wave forms.

NAND Gate	
NOR Gate	

Table (1)

In absence of any definite layout rules and primitives the exploration of every QCA based designs cannot function properly due to ignorance of electrostatic interference between closely placed paths, inputs and outputs. Some guidelines have been reported in [9] and although these can prove helpful in checking the noise interference to some extent but a universal design procedure guidelines need to be either incorporated in simulation software or declared after finding coincidence with the laboratory experimentation. Working with simulation techniques only we could see difference in waveform results of Exclusive-OR gate layout designs proposed by some researchers. While certain cases indicate presence of noise spikes and high propagation delays the others show results in complete disagreement. For analyzing the results of EX-OR layouts proposed in [10] and [12], we simulated the layouts again and the output waveforms were found in disagreement with the reported hypothesis. The simulation of one of the compact layouts reported in [11] for the design of parity checker has been observed to produce results in conformity with the projected reporting, although the latency is more due to incorrect clocking in the second stage of the layout. The circuit layout along with waveforms is given in Figure (8).

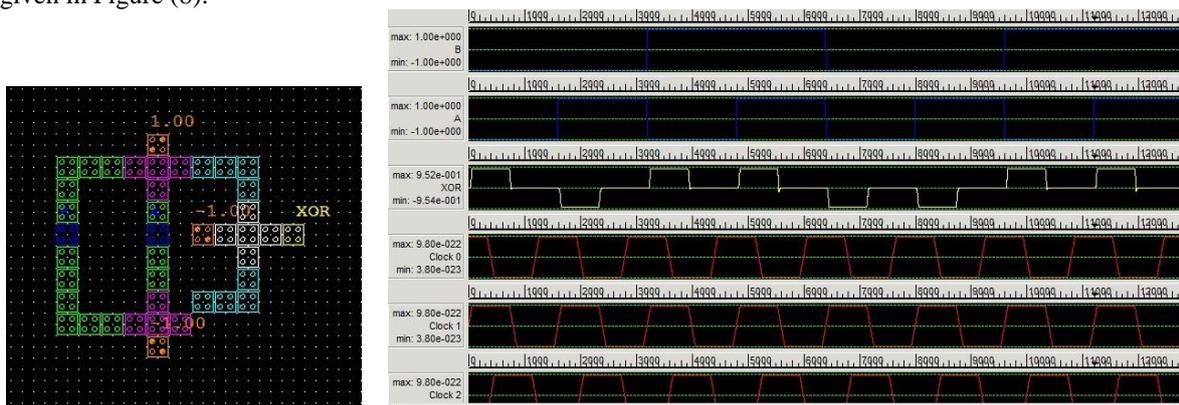


Figure (8)

An EX-OR gate layout has been reported in [13] for the design of half adder circuit and our analysis on simulations shows the results in agreement to the proposed claim. Although the NOT gate introduction at the input stage creates some noise spikes in the output waveforms but the layout is hypothetically behaving well under the QCA Designer simulation conditions. The design layout along with simulation result waveforms is presented in Figure (9). EX-OR layouts have been proposed by a number of researchers with simple one layer and complex multi-layer assemblies. In this paper we have only analyzed few single layer works as the analysis of proposed works is not possible and is also beyond our current study.

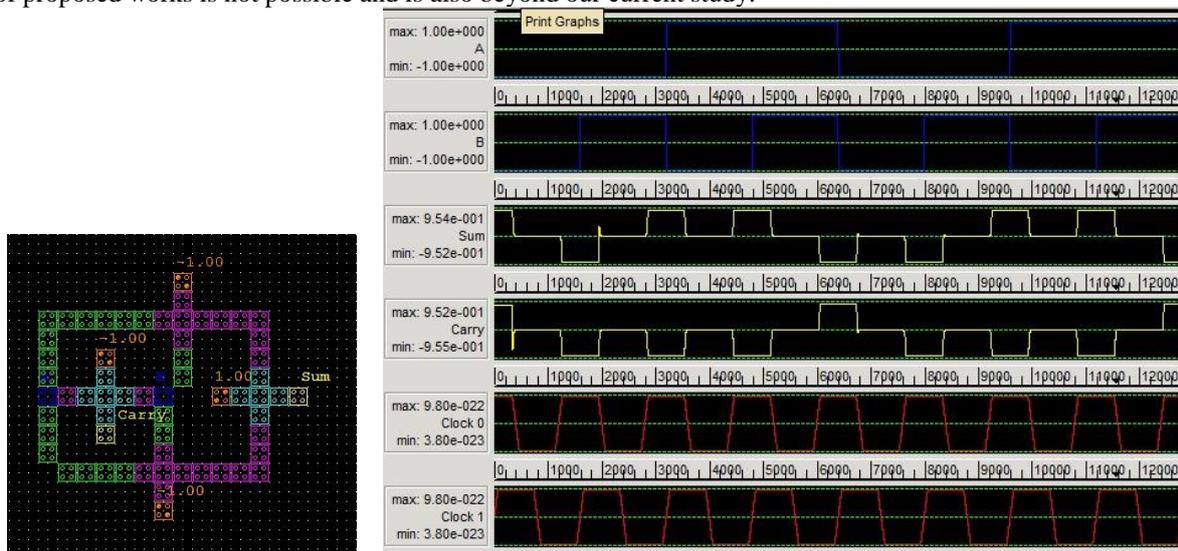


Figure (9)

Many reports suggest compact layout designs as a breakthrough but in absence of laboratory agreements one cannot be sure about the perfect implementation of these layouts due to presence of close inputs, outputs and paths. The electrostatic interference due to presence of various inputs around a single quantum cell and layout imbalance seems to be main cause for this undesired behavior. With the available simulation facilities we have tried to arrive at some agreement to propose few designs of the EX-OR gate that can be projected to have some valid benefits over the earlier works.

III. PROPOSED ADDER GATE DESIGNS

In the digital electronics the EX-OR gate is designed with the help of gate assemblies using Boolean Algebraic techniques. An EX-OR gate is producing a high output only when its two inputs are unequal. Hence a traditional gate is generally generated on the basis of this definition which is represented in the following Boolean expression:

$$Y = A\bar{B} + \bar{A}B \quad \dots (1)$$

The equation (1) can be expressed in different forms using simple Boolean Algebraic rules and is presented in the following transformations:

$$\begin{aligned} \bar{Y} &= \overline{A\bar{B} + \bar{A}B} \\ \text{Or } \bar{Y} &= (\overline{A\bar{B}}) \cdot (\overline{\bar{A}B}) \\ \text{Or } \bar{Y} &= (\overline{A + B}) \cdot (\overline{A + \bar{B}}) \\ \text{Or } \bar{Y} &= \overline{A\bar{A} + AB + \bar{A}\bar{B} + B\bar{B}} \\ \text{Since } \overline{A\bar{A} + B\bar{B}} &= 0 \quad \text{therefore} \\ \bar{Y} &= \overline{AB + \bar{A}\bar{B}} \\ \text{Or } \bar{Y} &= \overline{AB} \cdot \overline{\bar{A}\bar{B}} \\ \text{Or } Y &= (\overline{\overline{AB}}) \cdot (\overline{\overline{\bar{A}\bar{B}}}) \\ \text{Or } Y &= (\overline{\overline{AB}}) \cdot (\overline{\overline{A + B}}) \quad \dots (2) \\ \text{Or } Y &= (\overline{\overline{A + B}}) \cdot (\overline{\overline{A + B}}) \quad \dots (3) \end{aligned}$$

The equation (2) projects an EX-OR gate with the help of a NAND, an OR and an AND gates while as the equation (3) builds the same gate with the help of two OR, two NOT and an AND gate. There are other ways in which the gate can be constructed; few more expressions are given below for reference:

$$\begin{aligned} Y &= \overline{\overline{A \cdot (\overline{\overline{AB}})}} \cdot \overline{\overline{B \cdot (\overline{\overline{AB}})}} \quad \dots (4) \\ Y &= A \cdot (\overline{\overline{AB}}) + B \cdot (\overline{\overline{AB}}) \quad \dots (5) \\ Y &= \overline{\overline{AB}} + \overline{\overline{A + B}} \quad \dots (6) \end{aligned}$$

The analyzed layout of Figure (8) is based on the Boolean expression represented by equation (2) while as the layout of Figure (9) is implementation based on Boolean expression represented by equation (1). While exploring the implementation of EX-OR gate with the help of quantum cells the complexity of the representative equation is not our prime concern but the simplicity and balance of the layout. We have explored different expressions to reach the compact and simple arrangement of cells for robust implementation of the gate. The traditional gate implementation based on the Boolean expression represented by equation (1) is presented with a single layer layout design in Figure (10) along with simulation results.

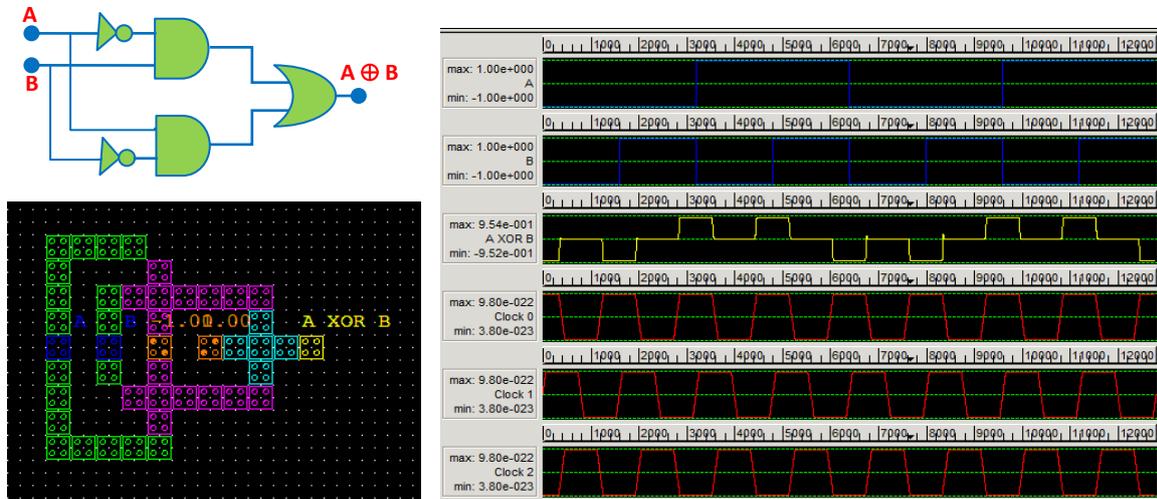


Figure (10)

The layout in Figure (10) is also based on the same expression but the proposed layout is improved with reduction cell count and has more balanced paths to improve the noise immunity. The layout took 10 seconds for simulation on QCA Designer and produced output after a propagation delay of approximately equal to half of the applied clock pulse. Another layout design of the gate based on the expression (2) was simulated and yielded results presented in Figure (11) along with its design and digital circuit diagram.

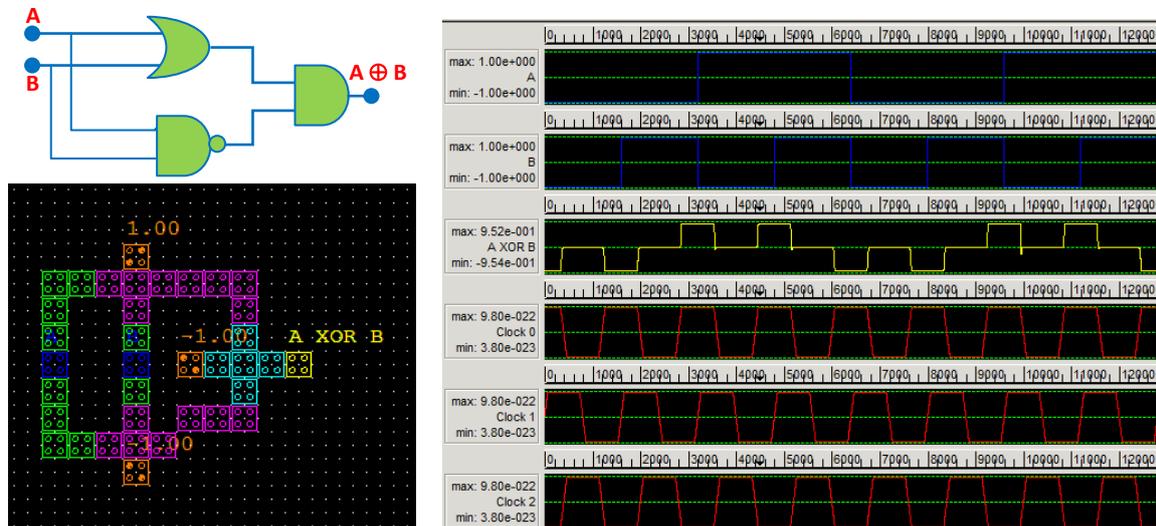


Figure (11)

The design analyzed above in Figure (11) is also based on the Boolean expression represented in equation (2) but has been improved in size, cell count, clocking and latency by us as may be clear from the performance comparisons in Table (2). This layout choice is versatile in various respects of quantum-dot cellular automata based view points. The additional features include, design of less complex half and full adder circuits, lesser cell count and minimum layout imbalance. Moving forward on the same considerations we have proposed one more layout for the gate based on Boolean expression represented by equation (6). The selection is not random as we have tried the other options as well but found the equation feasible for its lesser complexity and lower number of gate junctions. The layout along with digital gate representation and simulation results is presented in Figure (12). This layout is not only an improvement in size and cell count but has additional features of simple and easy conversion options to adders, logic comparators, parity checker/generators, and additive cellular automata based application circuit designs.



Figure (12)

The design advancement and performance features of the proposed adder gate layout assemblies are compared in Table (2) for ready reference to conclude this study.

Gate Layout/Result	Study Type	Latency in Clock Pulses	Cell Count	Area (μm^2)	Expression Reference
Figure (8)	Analysis	1.0 clock pulse	41	0.06	(2)
Figure (9)	Analysis	0.5 clock pulse	52	0.09	(1)
Figure (10)	Proposed	0.5 clock pulse	44	0.05	(1)
Figure (11)	Proposed	0.4 clock pulse	36	0.05	(2)
Figure (12)	Proposed	0.4 clock pulse	35	0.04	(6)

Table (2)

IV. CONCLUSION

In the pursuit of designing noise immune layouts for the EX-OR gate we have persuaded single layer assemblies to achieve the objectives. It is not only the reported primitives of crossovers, jogs and rippers but also an established parameter of balanced paths has been adopted to design the proposed layouts. The balanced path requirement which was found during this study is also an important element to cancel out the electrostatic noise. The noise reduction due to balanced paths is suggested cause for the cancellation of net noise and in absence of balanced paths there is an evident presence of noise spikes in the output waveforms. The layouts and the simulation results are not only clearly demonstrated but also analyzed for a clear understanding and facilitation of the future work.

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