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Modified Distributive Arithmetic Based DWT-IDWT Processor Design and FPGA Implementation for Image Compression

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Abstract: *One of the major image processing techniques that is widely used in medical, automotive, consumer and military applications is image compression. Discrete wavelet transforms is the most popular transformation technique adopted for image compression. Complexity of DWT is always high due to large number of arithmetic operations. In this work a modified Distributive Arithmetic based DWT architecture is proposed and is implemented on FPGA. The modified approach consumes area of 6% on Spartan-III pro FPGA and operates at 134 MHz. The modified DA-DWT architecture has a latency of 44 clock cycles and a throughput of 4 clock cycles. This design is twice faster than the reference design and is thus suitable for applications that require high speed image processing algorithms.*

Keywords: *Discrete Wavelet Transforms (DWT), Distributive Arithmetic (DA), Poly-phase structure, and convolution.*

I. Introduction

Technological growth of semiconductor industry has led to unprecedented demand for low power, high speed complex and reliable integrated circuits for medical, defence and consumer applications. Today's electronic equipment comes with user friendly interfaces such as keypads and graphical displays. As images convey more information to a user, it is many of the equipment today have image displays and interfaces. Image storage on these smaller, handled devices is a challenge as they occupy huge storage space; also image transmission requires higher bandwidth. Hence most of the signal processing technologies today has dedicated hardware that act as co-processors to compress and decompress images. In this work, a reliable, high speed, low power DWT-IDWT processor is designed and implemented on FPGA which can be used as a co-processor for image compression and decompression. The Discrete Wavelet Transform (DWT) is being increasingly used for image coding. This is because the DWT can decompose the signals into different sub-bands with both time and frequency information. It also supports features like progressive image transmission, compressed image manipulation, and region of interest coding [1]. Recently several VLSI architectures have been proposed to realize single chip designs for DWT [2]-[7]. Traditionally, such algorithms are implemented using programmable DSP chips for low-rate applications, or VLSI application specific integrated circuits (ASICs) for higher rates. In wavelet transforms, the original signal is divided into frequency resolution and time resolution contents. The decomposition of the image using 2-level DWT is shown in Figure 1.

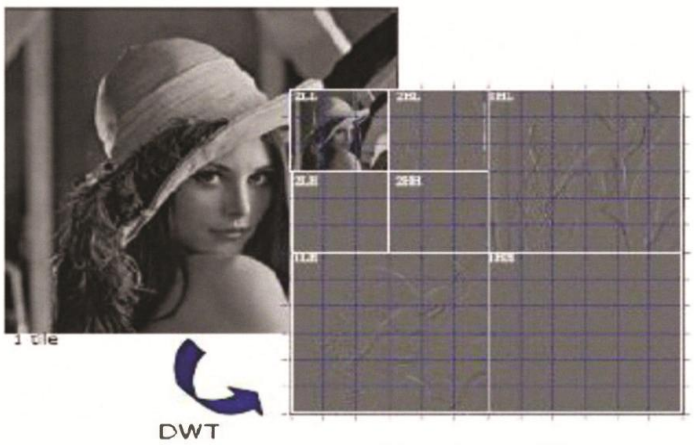


Figure 1: Decomposition of Image [8].

II. DWT Architecture

II. System Design Model

A. Dwt Architecture

Image consists of pixels that are arranged in two dimensional matrixes, each pixel represents the digital equivalent of image intensity. In spatial domain adjacent pixelvalues are highly correlated and hence redundant.

In order to compress images, these redundancies existing among pixels needs to be eliminated. DWT processor transforms the spatial domain pixels into frequency domain information that arerepresented in multiple sub-bands, representing different time scale and frequency points. Human visual system is very much sensitive to low frequency and hence, the decomposed data available in the lower sub-band region and is selected and transmitted, information in the higher sub-bands regions are rejected depending upon required information content. In order to extract the low frequency and high frequency sub-bands DWT architecture shown in figure below is used. As shown in the figure, input image consisting rows and columns are transformed using high pass and low pass filters. The filter coefficients are predefmed and depend upon the wavelets selected. In this work, 9/7 wavelets have been used for constructing the filters. First stage computes the DWT output along the rows, the second stage computes the DWT along the column achieving first level decomposition. Low frequency sub-bands from the first level decomposition is passed through the second level and third level of filters to obtain multiple level decomposition as shown in Figure 2.

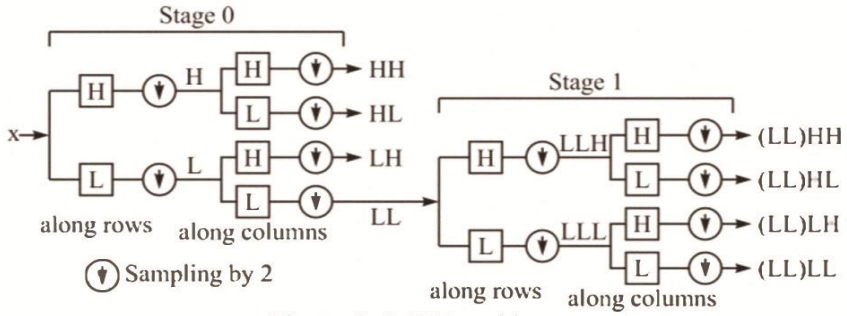


Figure 2: DWT architecture

There are several architectures for realizing the DWT shown in Figure 2, paper [11] summarizes various schemes. Most popular one is the DA-DWT scheme that is suitable on FPGA, as it consumes fewer resources and has high through put. DA-DWT architecture based on pipelining and parallel processing logic is realized and implemented on FPGA [12]. In this work, a modified DA-DWT architecture is designed based on the work reported in [12]. The number of LUTs and number of shift registers are reduced by exploiting the symmetric property of the 917 wavelet filters. Efficient fixed point number representation scheme is identified to accurately represent the 917 filter values and are stored in the LUT memory space on FPGA. A control logic designed loads the input data into the FPGA from the external memory, LUT contents are read out based on the input samples as address to LUT. After 8clock cycles of initial latency, DWT outputs are computed every clock cycle. A detailed discussion of the proposed architecture is presented in section IV. Software reference model for DWT-IDWT processor is built using Matlab. Multiple image test vectors are used in analysing the performances of the software reference model. A detailed discussion of the software reference model results are presented in section III.

B. Distributive Arithmetic Based 2D DWT/IDWT Architecture

In this section, we first outline how to perform multiplication by using memory based architecture. Following this, we briefly explain architecture for DWT filter bank. Using this we show complete design for block based DWT. The memory based approach provides an efficient way to replace multipliers by small ROM tables such that the DWT filter can attain high computing speeds with a small silicon area as shown in Figure 3.

Traditionally, multiplication is performed using logic elements such as adders, registers etc. However, multiplication of two n-bit input variables can be performed by a ROM table of size of 22n entries. Each entry stores the pre-computed result of a multiplication. The speed of the ROM lookup table is faster than that of hardware multiplication if the look-up table is stored in the on-chip memory. In DWT, one of the input variables in the multiplier can be fixed. Therefore, a multiplier can be realized by 2n entries of ROM. Distributed arithmetic implementation of the Daubechies 8-tap wavelet FIR filter consists of an LUT, a cascade of shift registers and a scaling accumulator [12].

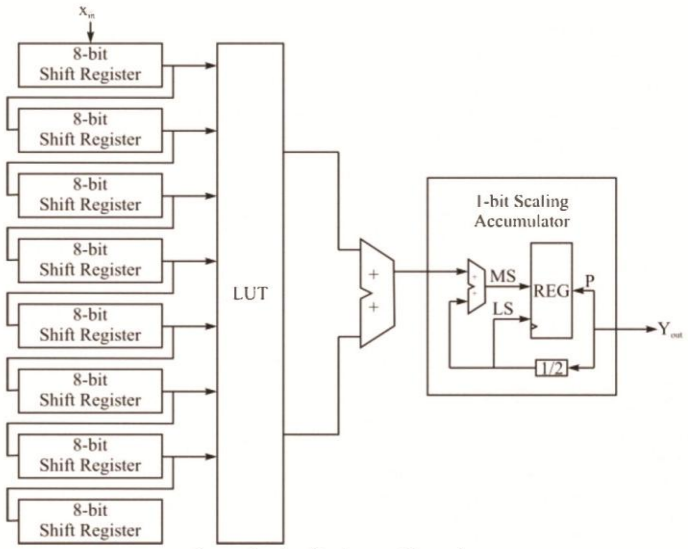


Figure 3 Distributive Arithmetic

To speed up the process parallel implementation of the Distributive Arithmetic (DA) architecture shown in Figure 4 is realized in [12]. In parallel implementation, the input data is divided into even samples and the odd samples based on their position. This scheme reduces the memory size to half due to the symmetric property of the filter coefficients. This increases the through put as the input samples are simultaneously used to read the data from two LUTs and hence speed is increased.

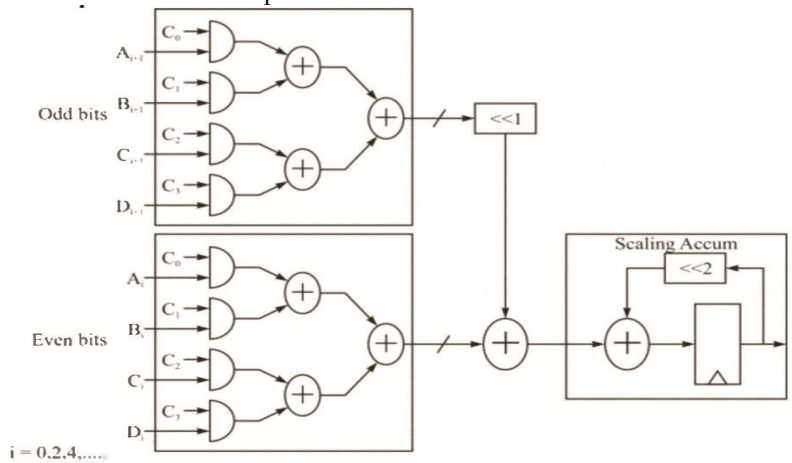


Figure 4 Parallel implementation of DA technique

In order to further increase the speed and reduce the area, the LUT can be further split into four stages, and can be accessed by the input values for data read.

IV. MODIFIED DA-DWT ARCHITECTURE

In order to further increase the speed and reduce the area, the LUT can be further split into four stages, and can be accessed by the input values for data read.

C. Modified DA-DWT architecture

The modified DA-DWT architecture shown in Figure 5 consists of four LUTs, each of the LUTs are accessed by the even and odd samples of input matrix simultaneously. Odd and even input samples are divided into 4 bits of LSB and 4 bits of MSB, each 4-bit data read the content of four different LUTs that consist of partial products of filter values computed and stored as per the DA logic. Input samples are split into even and odd in the first stage, the data is further loaded sequentially into the serial in serial out shift registers, top four shift register store MSB bits and bottom four shift register stores the LSB bits. It requires 40 clocks cycles to load the shift register contents. At the end of 40th clock cycle, the control logic configures the shift register as

serial in parallel out, thus forming the address for the LUT. The partial products stored in the LUT are read simultaneously front all 2 the four LUTS and are accumulated with previous values available across the shift register in the output stage. The output stage consisting of adders, accumulators and right shift registers are used to accumulate the LUT contents and thus compute the DWT output. This architecture has a latency of 44 clock cycles in computing the first high pass and low pass filter coefficient's, and has a through put of 4 clock cycles. This architecture is faster by the previous architectures as the latency is reduced by half clock cycles and through put is increased by a factor of 2.

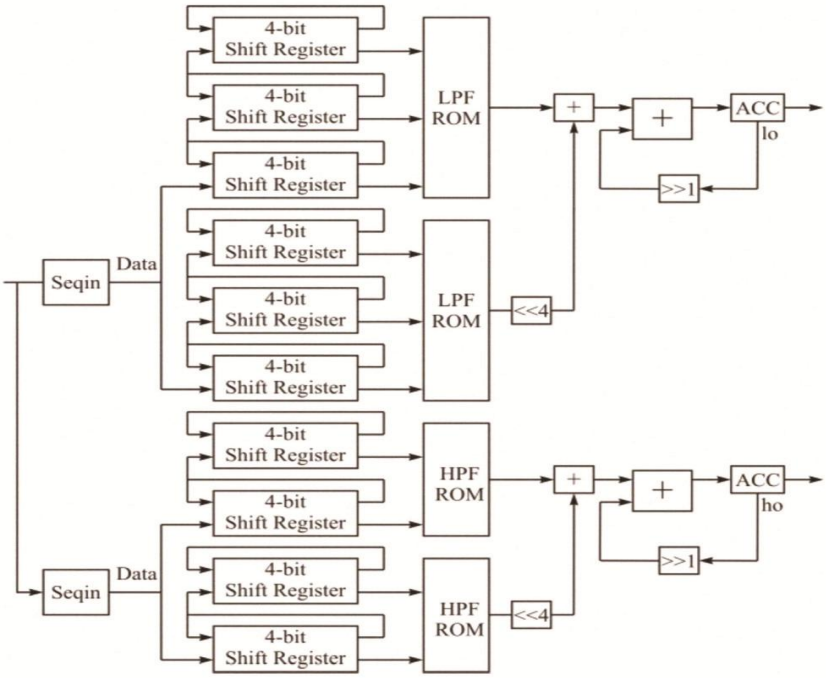
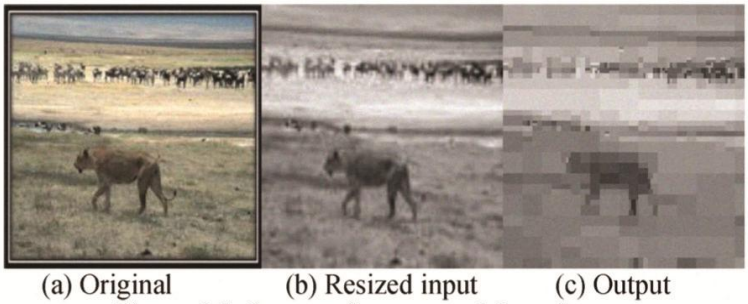


Figure 5 Practical Parallel implementation of DA technique

D. Software Reference Model Design

In this section, a software reference model is developed to analyse the performances of various wavelets for image compression using DA-DWT. Input image is rescaled into 100xlOO and is processed using DWT and IDWT algorithm. Decomposed sub-band components are selected to achieve different compression ratios. In this case, bits per pixels are used to express the compressed data. Bi-orthogonal, Haar and DB2 wavelets have been used to compare the performances of DWT-IDWT. Two test results have been shown in Figure 6. At very log bit BPP, the reconstructed image has lost the edges, this is due to the fact that very few sub-bands are chosen for reconstruction, hence data loss occurs.

MSE, Maximum error and PSNR are the three parameters that are used to analyse the DWT performances. The results of the same are shown in Table 1. From the results obtained, it is found that DB2 wavelet achieves better compression and also reconstruction is better in terms of MSE and PSNR. Based on these results, the hardware reference model is designed and developed.



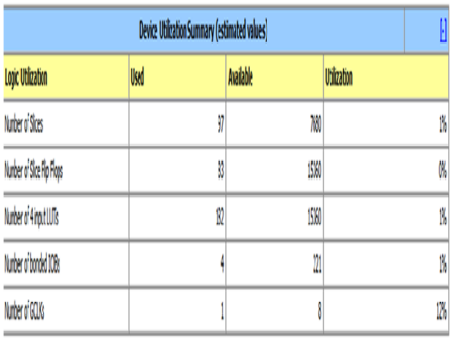
(a) Original (b) Resized input (c) Output

Figure 6 Software reference model results

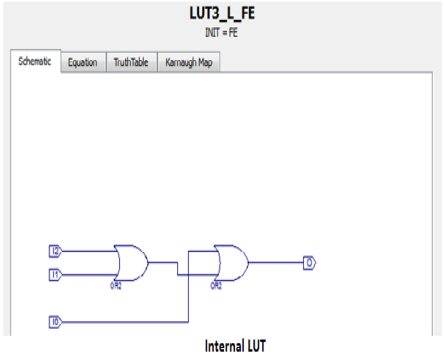
III. Fpga Implementation

HDL model for the proposed architecture is developed using Verilog. The developed model is simulated using test bench. The HDL model is synthesized using Xilinx ISE targeting Virtex II-pro FPGA. The proposed design is implemented and the synthesis report is generated. The results obtained are presented in Table 2. The proposed design implemented on FPGA occupies only 6% of the total slices on FPGA, thus the proposed architecture reduces the area by 30% compared to the earlier designs [12].

TABLE 2 SYNTHESIS REPORT



Synthesis report



Internal LUT

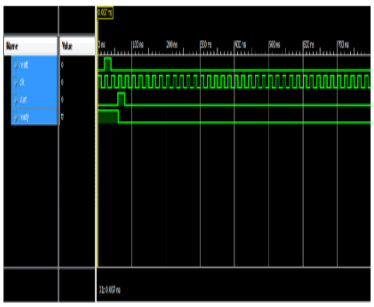
The proposed design IS optimized for timmg, and appropnate constraints are set for the best timing performances, the timing report is as follows:

- Speed Grade: -7
- Minimum period: 7.475ns (Maximum Frequency: 133.786MHz)
- Minimum input arrival time before clock: 2.226ns
- Maximum output required time after clock: 3.293ns

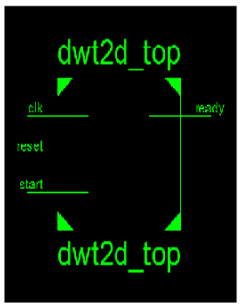
The device utilization is 6%, which implies that the design requires 1.8 million gates out of 30 million gates. This ensures that there is enough space for the further improvement and 3 also more space for multiple functions to be implemented on the selected FPGA. The maximum frequency at which the design works is at 134 MHz; this can be further improved by changing the architecture complexity.

IV. Simulation Results

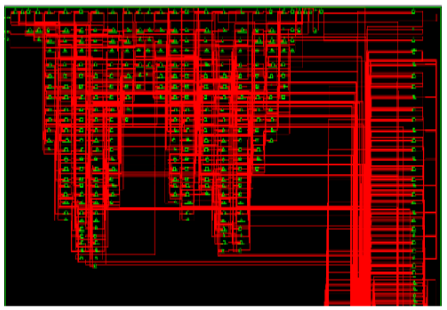
Model-Sim simulation results for the proposed design is presented in below array of figures. Input vectors that were obtained from MATLAB test inputs were used for validating the HDL results. Input vectors are stored in an ROM and are read into the modified DADWT architecture. The decomposed outputs are stored back and are also displayed using simulation waveforms. From theresults obtained and compared with MATLAB results it sound that the software and hardware results match and hence validates thefunctionality of the proposed approach.



Simulation of DWT IMAGE



Synthesis of DWT



RTL Schematic

V. Conclusions

The Discrete Wavelet Transform provides a multiresolution representation of images. The transform has been implemented using filter banks. For the design, based on the constraints the area, power and timing performance were obtained. Based on the application and the constraints imposed, the appropriate architecture can be chosen. For the Daubechies 2, the poly-phase architecture, with modified DA technique was implemented. The latency of the proposed architecture is 44 clock cycles and throughput is 4 clock cycles, and

hence is twice faster than the reference design. It is seen that, in applications, which require low area, power consumption, and high throughput, e.g., real-time applications, the poly-phase with DA architecture is more suitable. The biorthogonal wavelets, with different number of coefficients in the low pass and high pass filters, increase the number of operations and the complexity of the design, but they have better SNR than the orthogonal filters. First, the code was written in Verilog HDL and implemented on the FPGA using a 32 x 32 random image. Then, the code was taken through the ASIC design flow. For the ASIC design flow, 8x8 memory considered to store the image. This architecture enables fast computation of DWT with parallel processing. It has low memory requirements and consumes low power. By using the same concepts which are mentioned above are useful in designing the Inverse Discrete Wavelet Transform (IDWT).

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