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Comparative Analysis of Different Types of Full Adder Circuits

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Abstract: *The Full Adder circuit is an important component in application such as Digital Signal Processing (DSP) architecture, microprocessor, and microcontroller and data processing units. This paper discusses the evolution of full adder circuits in terms of lesser power consumption, higher speed. Starting with the most conventional 28 transistor full adder and then gradually studied full adders consisting of as less as 8 transistors. We have also included some of the most popular full adder cells like dynamic CMOS [9], Dual rail domino logic[14], Static Energy Recovery Full Adder (SERF) [7] [8], Adder9A, Adder9B, GDI based full adder.*

Keywords *: CMOS Transmission Gate (TG), Pass-Transistor Logic (PTL), Complementary Pass-transistor Logic (CPL), Gate Diffusion Input (GDI), Static Energy Recovery Full Adder (SERF), dynamic CMOS (D CMOS), Dual rail domino logic (DRD), Adder9A, Adder9B, GDI based full adder Power, Delay, Channel Length.*

I. Introduction

The core of every microprocessor, digital signal processor (DSP), and data processing application like specific integrated circuit (ASIC) is its data path. At the heart of data-path and addressing units in turn are arithmetic units, such as comparators, adders, and multipliers. Finally, the basic operation found in most arithmetic components is the binary addition. Computations needs to be performed using low- power, area-efficient circuits operating at greater speed. Addition is the most basic arithmetic operation; and adder is the most fundamental arithmetic component of the processor.The design criterion of a full adder cell is usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU). The limited power supply capability of present battery technology has made power consumption an important figure in portable devices.There is no ideal full adder cell that can be used in all types of applications [4]. Hence novel architectures such as CMOS Transmission Gate (TG), Pass-Transistor Logic (PTL), Complementary Pass-transistor Logic (CPL) [5],Dual rail domino logic[14] and Gate Diffusion Input (GDI) [6] are proposed to meet the requirements. Each design style has its own share of advantages and disadvantages. Gate Diffusion Input and Dual rail domino logic is a low power design that reduces transistor count. But the major problem of GDI is that it requires twin well CMOS or silicon on insulator (SOI) process for fabrication [11]. Thus GDI chips are more expensive. These logic styles and their combinations (Hybrid) are commonly used in designing full adder cells.

The rest of the paper is organized as follows. Section II describes the truth table and equation. Section III elaborates the different types of full adder circuits. Section IV and V are followed by schematic diagram of full adder and simulation result. Finally, section VI concludes the work.

II. Truth Table And Equation

Addition is a fundamental operation for any digital system, digital signal processing or control system. A fast and accurate operation of a digital system is greatly influenced by the performance of the resident adders because of their extensive use in other basic digital operations such as subtraction, multiplication and division.

The conventional logic equation for Sum and Carry are [3]: Sum = C ex-or (A ex-or B)
Carry = (A and B) or C(A ex-or B)

III. Different Types of Full Adder Circuits

In this section the different types of full adder circuits are discussed.

A. Conventional 28T CMOS Full Adder Circuit

The conventional CMOS [14] adder cell using 28 transistors based on standard CMOS topology is shown in fig.1. Due to high number of transistors, its power consumption is high. Large PMOS

transistor in pull up network result in high input capacitances, which cause high delay and dynamic power. One of the most significant advantages of this full adder was ts high noise margins and thus reliable operation at low voltages.

B. 14 T Full Adder Circuit

The 14T full adder contains a 4T PTL XOR gate, shown in Fig. 3, an inverter and two transmission gates based multiplexer designs for sum and Cout signals[11]. This circuit compared with the previous 10-transistor full adders and the conventional 28-transistor CMOS adder [13].

F. Transmission Gate Full Adder Circuit

20 T transmission produces buffered outputs of proper polarity for both sum and carry. (Fig.3). In this circuit 2 inverters are followed by two transmission gates which act as 8-T XOR. Subsequently 8-T XNOR module follows. To has 4 transistor XOR which in the next stage is inverted to produce XNOR. These XOR and XNOR are used generate sum; **cin** and C_{in} are multiplexed which can simultaneously to generate sum and cout. The signals cin controlled either by (**a b**) or (**a** $\otimes$ **b**).Similarly the cout can be calculated by multiplexing **a** and **cin** which is controlled by (**a)**and C_{in} are multiplexed which can controlled either by (a b) **b**). The power dissipation in this circuit is more than the 28T or (a $\otimes$ b). Similarly the cout can be calculated by multiplexing a and cin controlled by (a b). The power dissipation in this circuit is more than the 28T adder. However with same power consumption it performs faster [4].

C. 8 T Full Adder Circuit

The basic of 8T full adder consists of 3 modules: 2 XOR elements and a Carry section as shown in fig.5.The Sum output is obtained by two XOR blocks in succession. For the carry section GDI based 2TMUX is used and (A XOR B) as the selection signal. The Sum and the Cout module need 6 and 2 transistors respectively. The transistor level implementation of the eight transistor full adder is shown in Fig. 8. It is obvious from the figure that both Sum and Cout has a maximum delay of 2T. It doesn't suffer from threshold voltage loss problem. Also the noise margin has been substantially increased by proper sizing of transistors in 3T XOR. The power delay product (PDP), and the area of the proposed adder are also found better than that of the existing 10T and 14T adders. Higher power consumption due to short circuit current.

D. 12T Full Adder Circuit

MB12T [15] has been implemented using six multiplexers and 12 transistors. Each multiplexer is implemented by pass- transistor logic with two transistors. As shown in Fig. 10, there is no VDD or GND connection in this circuit and there are some paths containing three serried transistors. It causes to increase delay of producing SUM signal. The size of each transistor in mentioned path should be three times larger to balance the output and optimize the circuit for PDP. Therefore, the area of the circuit is increased.

E. ADDER 9A AND 9B

The Static Energy Recovery XNOR gate is cascaded with the new G-XNOR gate to generate the Sum while the Cout function is implemented by simply multiplexing B and Cin controlled by (A XNOR B) as done in the previous circuits. (Fig 7 and 8). These two new adders consistently consume less power in high frequencies and have higher speed adder. However with same power consumption it performs faster [8].

G. Static Energy Recovery Full Adder Circuit

In the 10T adder cell, the implementation of XOR and XNOR of A and B is done using pass transistor logic and an inverter is to complement the input signal A. This implementation results in faster XOR and XNOR outputs and also ensures that there is a balance of delays at the output of these gates. This leads to less spurious SUM and Carry signals (Fig 6). The energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic.

Advantage: It should be noted that the new SERF adder has no direct path to the ground. The elimination of a path to the ground reduces power consumption. The charge stored at the load capacitance is

reapplied to the control gates. The combination of not having a direct path to ground and the re-application of the load charge to the control gate makes the energy-recovering full adder an energy efficient design[12].

Disadvantage: The circuit produces full-swing at the output nodes. But it fails to provide so for the internal nodes. As the power consumption by the circuit reduces the circuit becomes slower. Also it cannot be cascaded at low power supply due to multiple threshold problems [12].

H. GDI Structure Based Full Adder Circuit

A new low power design technique that solves most of the problems known as Gate-Diffusion-Input (GDI) is proposed. This technique allows reducing power consumption, propagation delay, and area of digital circuits. A basic GDI cell contains four terminals – G (common gate input of nMOS and pMOS transistors), P (the outer diffusion node of pMOS transistor), N (the outer diffusion node of nMOS transistor), and D (common diffusion node of both transistors).GDI method is based on the use of a simple cell as shown in figure 2. At the first look the design is seems to be like an inverter, but the main differences are 1) GDI consist of three inputs- G (gate input to NMOS/PMOS), P (input to source of PMOS) and N (input to source of NMOS). (2) Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter.This design can implement a wide variety of logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors ,while improving logic level swing and static power characteristics and allowing simple top-down design by using small cell library(Fig. 12).

I.Dual Rail Domino Full Adder Circuit

Dual-Rail Domino Logic is a precharged circuit technique [7] which is used to improve the speed of the CMOS circuits. Figure.10 shows a Dual-Rail Domino full adder cell. A domino gate consists of a dynamic CMOS circuit followed by a static CMOS buffer. The dynamic circuit consists of a pMOSFET precharge transistor and an nMOSFET evaluation transistor with clock signal (CLK) applied to their gate nodes, and an nMOSFET logic block which implements the required logic function.[1] During the precharge phase (CLK=0) the output node of the dynamic circuit is charged through the precharged PMOSFET transistor to supply voltage level. The output of the static buffer is discharged to ground. During evaluation phase (CLK=1) the evaluation nMOSFET logic block, the output of the dynamic circuit is either discharged or it will stay precharged. Since in dynamic logic every output node must be precharged every clock cycle, some nodes are precharged only to be immediately discharged again as the node is evaluated, leading to higher switching power dissipation.One major advantage of dynamic, precharged design styles over the static styles over the static styles is that they eliminate the spurious transitions and the corresponding power dissipation.[5][7] Also, dynamic logic doesn't suffer from short-circuit currents which flow in static circuits when a direct path from power supply to ground is caused. However, in dynamic circuits, additional power is dissipated by the distribution network and the driver of the clock signal. Schematic of Dual-Rail domino full adder circuit is as shown in Fig.(9).

J. Conventional Dynamic Full Adder Circuit

The conventional dynamic full adder cell [1] has 16 transistors and is based on NP-CMOS logic style (Fig. 10).

IV. Schematic Diagrame Of Different Full Adder Circuits

TABLE I
TRUTH TABLE OF FULL ADDER

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

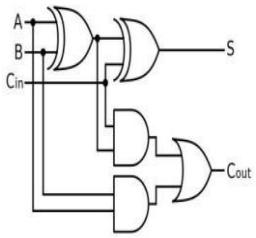


Fig 1: Block Diagram of Basic Full Adder

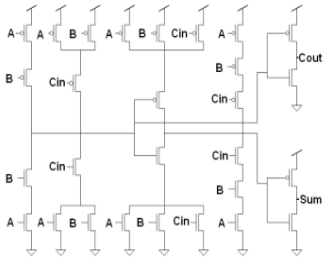


Fig 2 : 28T Conventional CMOS Full Adder

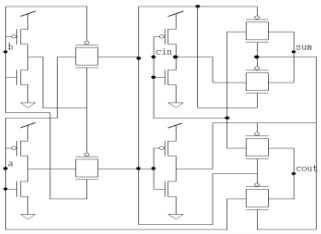


Fig 3**: Transmission Gate Full Adder**

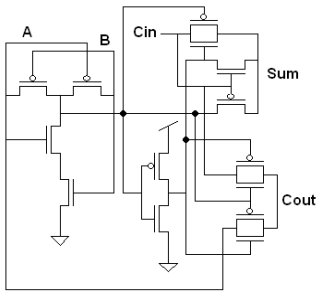


Fig 4: *14T Full* Adder

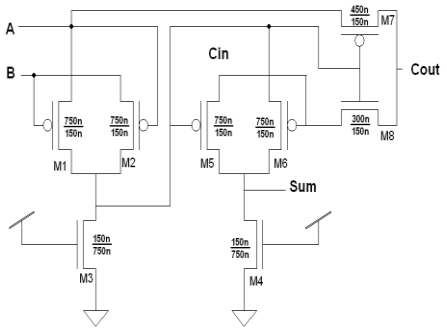


Fig 5 : 8 T Full Adder

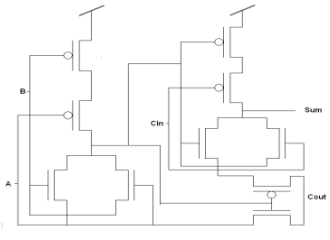


Fig 6 : SERF Full Adder

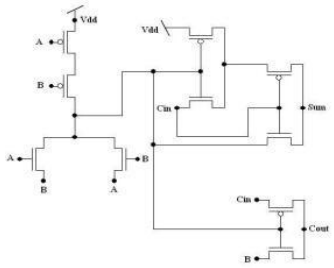


Fig 7: Adder 9A

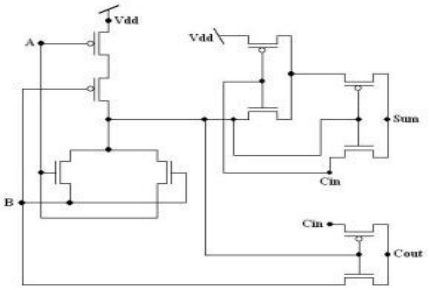


Fig 8: Adder 9B

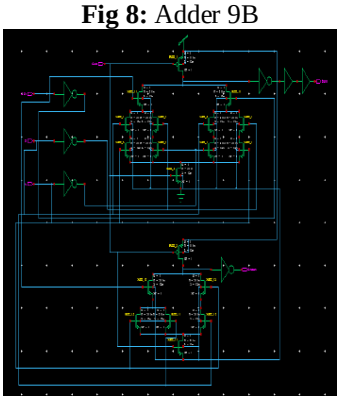


Fig 9: Schematic of Dual-Rail Domino full adder

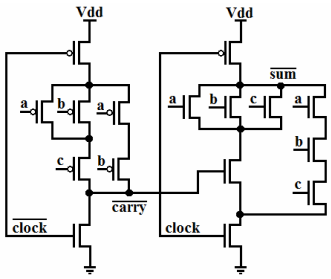


Fig 10: Conventional Dynamic Full Adder

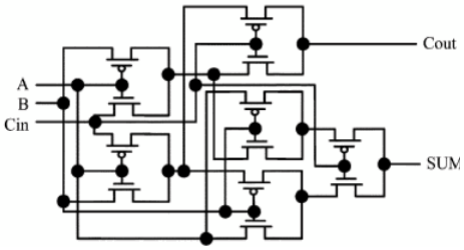


Fig 11: 12 T Full Adder

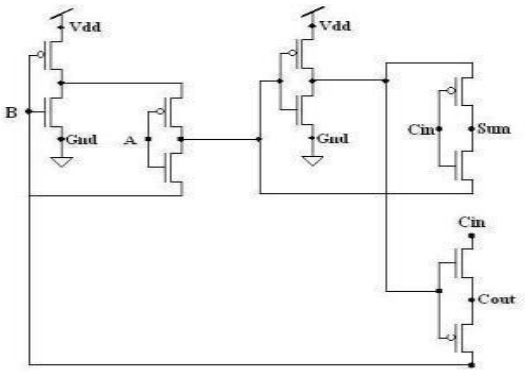


Fig 12: GDI Structure Based Full Adder

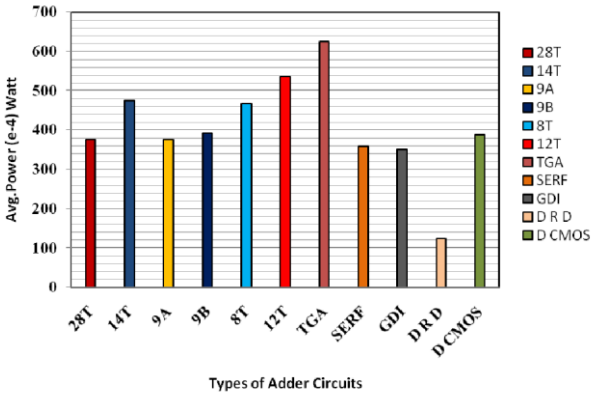
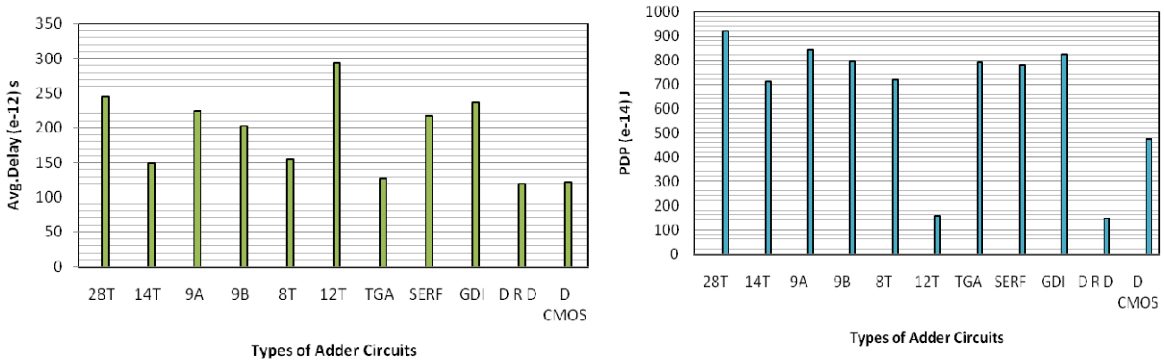


Fig 13: **Power of the different Full Adder Cells Fig 14**: **Delay of the different Full Adder Cells Fig 15: PDP of the different Full Adder Cells**

V. Simulation Result

The most conventional 28 transistor full adder, 14T, 8T ,12T, and the other conventional full adder cells (dynamic CMOS, Dual rail domino logic, Static Energy Recovery Full Adder (SERF), Adder9A, Adder9B, GDI based full adder.) are all simulated using TSpise and 180nm CMOS technology at room temperature. Because of dynamic logic characteristic, the inputs should be changed in precharge/predischarge phase and the results are obtained during evaluation phase. The delay parameter is calculated from the time that the clock



signal reaches 50% of the supply voltage level, to the time that the output reaches the same voltage. The average power consumption during all the transitions is considered as the power consumption parameter. Finally the power-delay product (PDP) is the multiplication of the maximum delay and the average power consumption.

Table II
Comparative analysis of various type of
Full Adder

Parameter	28T	14T	9A	9B	8T	12T
Avg. Power (e-4)Watt	376.18	475.89	375.9	392.6	466.6	535.5
Avg. Delay (e-12)Watt	244.92	149.98	224.3	202.6	154.15	293.7
PDP(e-14)J	921.34	713.74	843.2	795.5	719.96	157.2

Table II
Comparative analysis of various type of
Full Adder

Parameter	TGA	SERF	GDI	Dual Rail Domino	Dynamic CMOS
Avg. Power (e-4)Watt	624.99	359.04	349.89	123.37	389.12
Avg. Delay (e-12)Watt	126.72	216.81	235.97	120	122.45
PDP(e-14)J	792.04	778.43	825.64	148.04	476.47

The results are shown in Table I and Table II at 1.8v. Figure
13, figure 14 and figure 15 shows the avg. power, avg. delay and PDP of different full adder circuits respectively. Figure 11 shows the minimum power dissipation (123.37e-4Watt) for dual rail domino logic while maximum power dissipation (624.99 e-4Watt) for the transmission gate based full adder circuit. Figure 12 shows the minimum avg. delay 120ps for dual rail domino logic and 123ps for the transmission gate based full adder circuit. Finally figure 13 shows the PDP of different full adder circuits, which shows the minimum PDP for dual rail domino logic as well as for 12T full adder circuit.

VI. Conclusion

From the analysis of the above various type of Full Adder Circuits. It can be concluded that the average power is low for Dual Rail Domino Logic type Full adders and Average Delay is low for TG Based Full Adder as well as for Dual Rail Domino Logic type Full adders. But the Power Delay Product is low for Dual Rail Domino Logic type Full adders

Full Adders is the heart of any digital and data processing application like specific integrated circuit (ASIC) is its data path. At the heart of data-path and addressing units in turn are arithmetic units, such as comparators, adders, and multipliers. Finally, the basic operation found in most arithmetic components is the binary addition. Addition is the most basic arithmetic operation; and adder is the most fundamental arithmetic component of the processor. This paper presents the implementation of various type of Full Adders using MOSFET and concluded that the dual rail domino logic based full

adder circuit is fit for delay and power centric design.

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References

[1] Chandrakasan, R. Brodersen, "Low Power Design", Kluwer Academic Publishers, 1995.
[2] A. M. Shams, and M. A. Bayoumi, "A Novel High Performance CMOS 1-Bit Full Adder Cell", IEEE Transactions on Circuit and System, vol.47, NO. 5,May, 2000.
[3] J. H. Kang and J. B. Kim, "Design of a Low Power CVSL Full Adder Using Low-Swing Technique", ICSE2004 Proc. 2004, Kuala Lumpur, Malaysia.
[4] A. A. Khatibzadeh and K. Raahemifar, "A Study and Comparison of Full Adder Cells based on the Standard Static CMOS Logic.", IEEE CCECE 2004 -CCGEI 2004, Niagara Falls, May 2004.
[5] S. M. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Third Edition, Tata McGraw-Hill Edition 2003, pp 307-316.
[6] A. Morgenshtein, A. Fish and A. Wagner, "Gate-Diffusion Input(GDI): A Power-Efficient Method for Digital Combinational Circuits", IEEE Trans.VLSI Syst., pp. 566-581, Oct. 2002.
[7] I. Hassoune, D.Flandre, I. O'Connor and J. D. Legat, "ULPFA: a new efficient design of a power aware full adder", IEEE Transactions on Circuits andSystems I-5438, 2008.
[8] R. Zimmermann and W. Fichter, "Low –power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid-State Circuits, Vol. 32, July 1997,pp.1079-90
[9] N. Weste and K. Eshraghian, "Principles of VLSI Design, A System Perspective", Reading, MA: Addison-Wesley, 1993.
[10] N. Zhuang and H. Wu, "New Design of the CMOS Full Adder", IEEE J. Solid-State Circuits, vol. 27,no. 5,pp. 840-844, May 1992
[11] J. Wang, S. Fang, and W. Feng, "New efficient designs for XOR and XNOR functions on the transistor level", IEEE J. Solid-State Circuits, vol. 29, no. 7,Jul. 1994, pp. 780–786.
[12] R. Shalem, E. John, and L. K. John, "A Novel Low Power Energy Recovery Full Adder Cell" in Proc. IEEE Great Lakes VLSI Symp., pp. 380–383, Feb.1999.
[13] H. T. Bui, A. K. Al-Sheraidah and Y. Wang, "Design and Analysis of 10-transistor Full Adders using Novel XOR-XNOR Gates" , Proceedings of ICSP2000.
[14] P. M. Lee, C. H. Hsu, and Y. H. Hung, "Novel 10-T full adders realized by GDI structure" IEEE International Symposium on Integrated Circuits (ISIC-2007).
[15] J. F. Lin, Y. T. Hwang, M. H. Sheu and C. C. Ho, "A novel High- Speed and Energy Efficient 10-Transistor Full Adder Design", IEEE Transactions on Circuits and System—I: Regular Papers, VOL. 54, NO. 5, May 2007.
[16] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," in Proc. IEEE Circuits Devices Systems, vol. 148, FEB 2001, pp 19-24.
[17] S. Goel, A. Kumar, M. A. Bayoumi, "Design of Robust, Energy- Efficient Full Adders for Deep-Submicrometer Design Using Hybrid- CMOS Logic",IEEE Transactions on VLSI 2006
[18] J. F. Lin, Yin-Tsung Hwang, Ming-Hwa Sheu, and Cheng-Che Ho,May 2007. "A Novel High-Speed and Energy Efficient 10- Transistor Full Adder Design," IEEE Trans. On circuits and systems-I, VOL. 54,NO.5,PP.1050-1059.
[19] Navi, K., M. Maeen, V. Foroutan, S. Timarchi and O. Kavei, 2009. "A novel low power full-adder cell for low voltage," Integration the VLSI J., 42(4): 457-467.
[20] Ghadiry, M.H., Abu Khari A'Ain and M. Nadisenejani, 2011. "Design and analysis of a novel low PDP full adder cell," Submitted for publication in J. Circuits, Systems and Computers, pp: 20(3).
[21] Navi, K., M. Maeen, V. Foroutan, S. Timarchi and O. Kavei, 2009. "A novel low power full-adder cell for low voltage," Integration the VLSI J., 42(4): 457-467.
[22] Investigating the Impact of Logic and Circuit Implementation on Full Adder Performance, Sohan Purohit and Martin Margala,IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 20, NO. 7, JULY 2012
[23] Sreenivasa Rao.Ijjada, Ayyanna.G , G.Sekhar Reddy, Dr.V.Malleswara Rao, PERFORMANCE OF DIFFERENT CMOS LOGIC STYLES FOR LOW POWER And HIGH SPEED, International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.2, June 2011
[24] B. Ramkumar and Harish M Kittur, Low-Power and Area-Efficient Carry Select Adder, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 20, NO. 2, FEBRUARY 2012

Biography

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