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Design Of FFT Using ALU For Efficient OFDM Systems

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Abstract- *In present scenario every process should be efficient and simple. Fast Fourier Transform (FFT) is an efficient algorithm to compute the N point DFT. The main focus of this paper is to design FFT using ALU which is used in receiver blocks of OFDM system. It has greater applications in signal and image processing, communication and instrumentation. But the design of FFT requires large number of additions and complex multiplications. To make this process rapid and simple, the FFT operation should be faster and power efficient. Hence, the 64-point FFT is designed using Arithmetic Logic Unit (ALU).It requires less power compared to the FFT designed using Decimation in Time (DIT) butterfly structure. The design is done in HDL and the synthesized results are analyzed using Xilinx ISE tool.*
Keywords- *ALU,DIT, FFT,IFFT,OFDM.*

1. Introduction

The fast growth in multimedia applications involve more and more transmissions of graphical data, video and audio messages. In modern communication systems, Orthogonal Frequency Division Multiplexing (OFDM) systems are used to transmit with higher data rate and avoid Inter Symbol Interference (ISI) .In an OFDM communication system, the broadband is partitioned into many orthogonal sub-carriers, in which data is transmitted in a parallel fashion. Thus the data rate for each sub-carrier is lowered by a factor of N in a system with N sub-carriers. By this method, the channel is divided into many narrowband flat fading sub-channels. This makes the OFDM system more resistant to the multi-path frequency selective fading than the single carrier communication system. The sub-carriers are totally independent and orthogonal to each other. The sub-carriers are placed exactly at the nulls in the modulation spectral of one another. At the peak point of one sub-carrier waveform, the sample values of other sub-carriers at the nulls are zeros and thus contribute no ISI to the sampled sub-carrier The OFDM transmitter and receiver contain Inverse Fast Fourier Transform (IFFT) and Fast Fourier Transform (FFT), respectively. The IFFT/FFT algorithms [7] are chosen due to their execution speed, flexibility and precision. Fast Fourier transform (FFT) is an efficient implementation of the discrete Fourier transform (DFT). This paper concentrates on the development of the Fast Fourier Transform (FFT) using Arithmetic Logic Unit (ALU). My paper uses VHDL as a design entity, and Synthesis by Xilinx Synthesis Tool. The rest of the paper is organized as follows: Section 2 discusses the theoretical information. Section 3 describes the proposed work. Section 4 describes the simulation environment and presents the simulation results. Section 5concludes the paper and lists the future work.

2. Theoretical information

In this Section, a brief overview of FFT algorithm is given and it is efficiently used in OFDM systems. FFT algorithm is based on a specific mathematical equation array. Certain data that are being obtained from a signal are replaced in these equations to count DFTs and owing to these equations; processes are counted very fast than normal DFT equation[3].

2.1. Fast Fourier Transform

The Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT) are derived from the main function, which is called Discrete Fourier Transform (DFT). In DFT, the computation for N-points of the DFT will be calculated one by one for each point. While for FFT/IFFT, the computation is done simultaneously and this method saves quite a lot of time.

FFTs are of great importance to a wide variety of applications, from digital signal processing and solving partial differential equations to algorithms for quick multiplication of large integers. The best-known FFT algorithms depend upon the factorization of *N*, but there are FFTs with O(*N* log *N*) complexity for all *N*, even for prime N.

An FFT computes the DFT and produces exactly the same result as evaluating the DFT definition directly; the only difference is that an FFT is much faster. (In the presence of round off error, many FFT algorithms are also much more accurate than evaluating the DFT definition directly. Evaluating this definition directly requires O(N^2) operations: there are *N* outputs X_k, and each output requires a sum of *N* terms. An FFT is any method to compute the same results in O(*N* log *N*) operations. More precisely, all known FFT algorithms require $\underline{\Theta}$(*N* log *N*) operations.

2.2. Arithmetic Logic Unit (Alu)

An arithmetic-logic unit (ALU) is the part of a computer processor (CPU) that carries out arithmetic and logic operations on the operands in computer instruction words. Arithmetic units are usually grouped together into an ALU which has inputs, outputs, and control bits which tell the ALU which type of operation to perform. Figure 1.4 shows a typical diagram of an ALU. In this diagram A and B are the data inputs, F is the control input to choose the function, R is the result of the function applied to A and B, and D is the status of the output so that you know when the function is done.

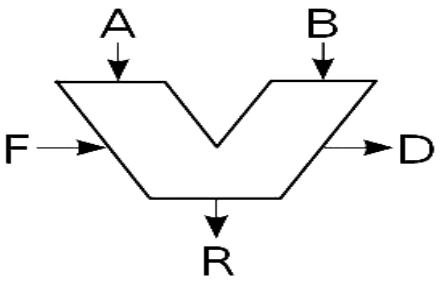

Figure 1: A typical ALU

3.Proposed Work

OFDM systems rely on the FFT for an efficient implementation of the signal demodulation on the receiver side. The FFT becomes one of the most critical module in OFDM transceivers. The Fast Fourier Transform (FFT) is a computationally intensive digital signal processing (DSP) function widely used in applications such as imaging, software-defined radio, wireless communication, instrumentation. In this project, a reconfigurable FFT design using Arithmetic Logic Unit with high speed and small area is presented.

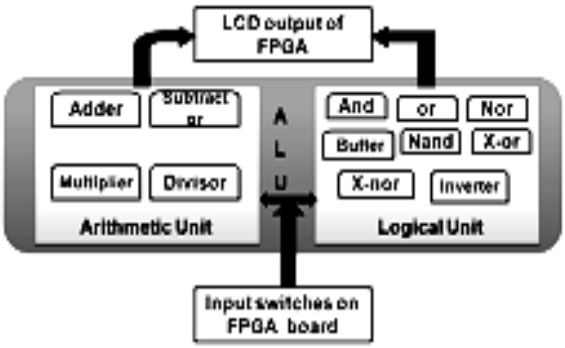

Figure 2: Block Diagram of ALU

Fast Fourier transform (FFT) is an efficient algorithm to compute the N point DFT. But the Implementation of FFT requires large number of complex multiplications, so to make this process rapid and simple it's necessary for a multiplier to be fast and power efficient. Proposed system implementing FFT using Arithmetic

Logic Unit with ripple carry adder, subtractor and normal multiplier. The Fast Fourier Transform(FFT) is designed using Arithmetic Logic Unit. It consist of 8-bit ripple carry adder, 8-bit subtractor and 8-bit normal multiplier for the design of 8 point FFT. Similarly 64-bit ripple carry adder, 64-bit subtractor and 64-bit normal multiplier is used to design of 64 point FFT.

3.1. 8- Point FFT

In digital signal processing to perform different types of operations we use various algorithms , out of these algorithms Fast Fourier Transform (FFT) is the most important and significant algorithm**.**Basically the FFT algorithm is used as an efficient means to compute the DFT and IDFT. The FFT algorithm is used in variety of areas, including linear filtering, correlation and spectrum analysis, because of its capability to perform efficient computation in comparison to the DFT. There are mainly two ways, through which FFT algorithm can be performed, which are DIT and DIF whose acronyms are Decimation In Time and Decimation In Frequency respectively. Speed of both of these FFT algorithms mainly rely on the multiplier used in it. So performance of FFT processor can enhanced with the use of highly speed efficient multiplier. And in direction to achieve this goal of designing Speed efficient FFT processor, the FFT is designed using ALU.

3.2. 64- Point FFT

OFDM systems rely on the IFFT for an efficient implementation of the signal modulation on the transmitter side, whereas the FFT is used for efficient demodulation of the received signal.

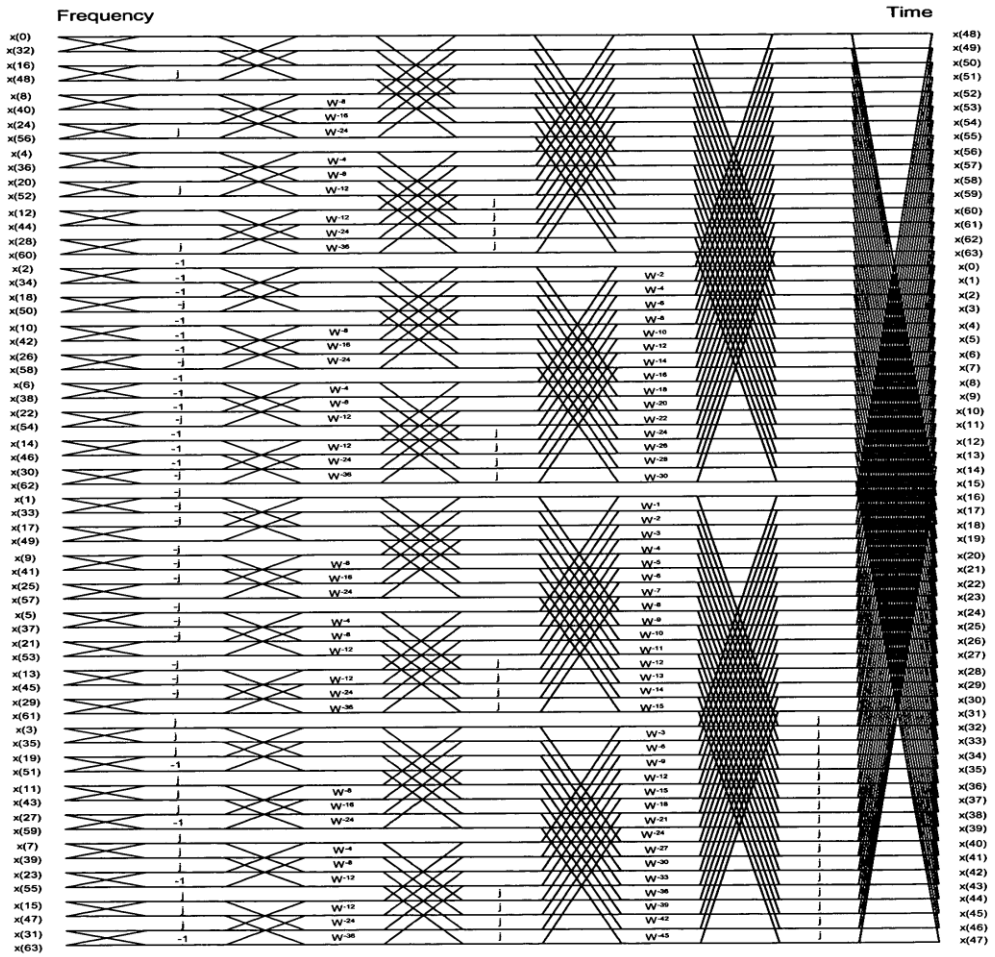

Figure 3: 64- Point FFT

The FFT/IFFT becomes one of the most critical modules in OFDM transceivers. In fact, the most computationally intensive parts of an OFDM system are the FFT in the transmitter and the Viterbi decoder in the receiver Therefore, the implementation of the FFT must be optimized to achieve the required throughput with the minimum penalty in area and power consumption. The demanding requirements of modern OFDM transceivers lead, in many cases, to the implementation of special–purpose hardware for the most critical parts of the transceiver. Thus, it is common to find the FFT implemented as a Very Large Scale Integrated (VLSI) circuit.

4.Simulation Results

The simulation results for FFT block is shown in the following figures. The simulation waveform is obtained for 8-pt FFT and 64-pt FFT using ALU. The various output is obtained by varying the input values.

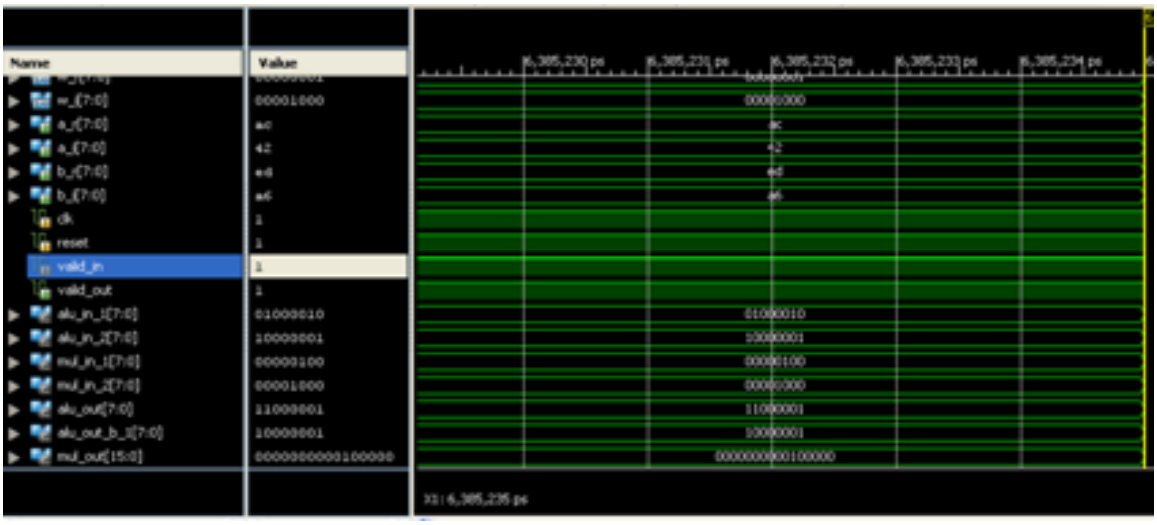

Figure 4: simulation waveform of 8-pt FFT using ALU

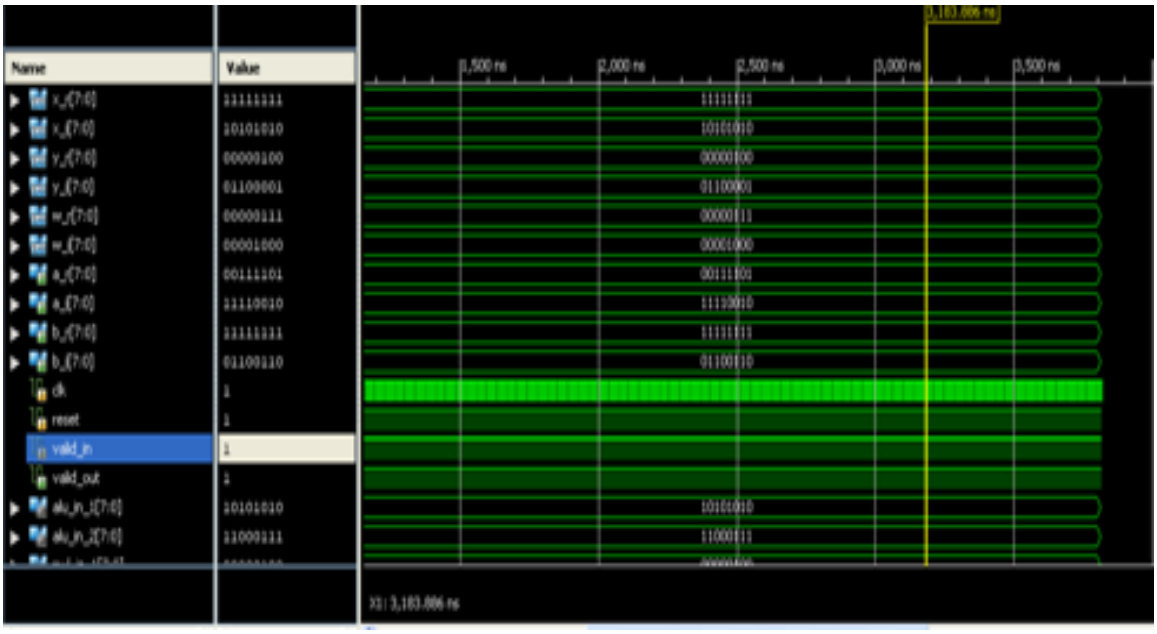

Figure 5: simulation waveform of 8-pt FFT using ALU

Figure 6:simulation waveform of 64-pt FFT using ALU

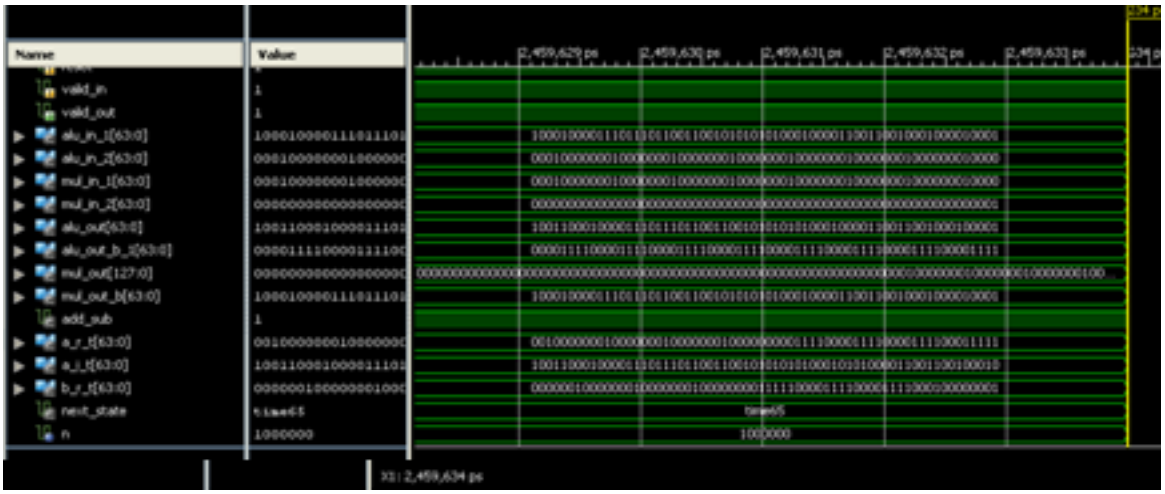

Figure 7: simulation waveform of 64-pt FFT using ALU

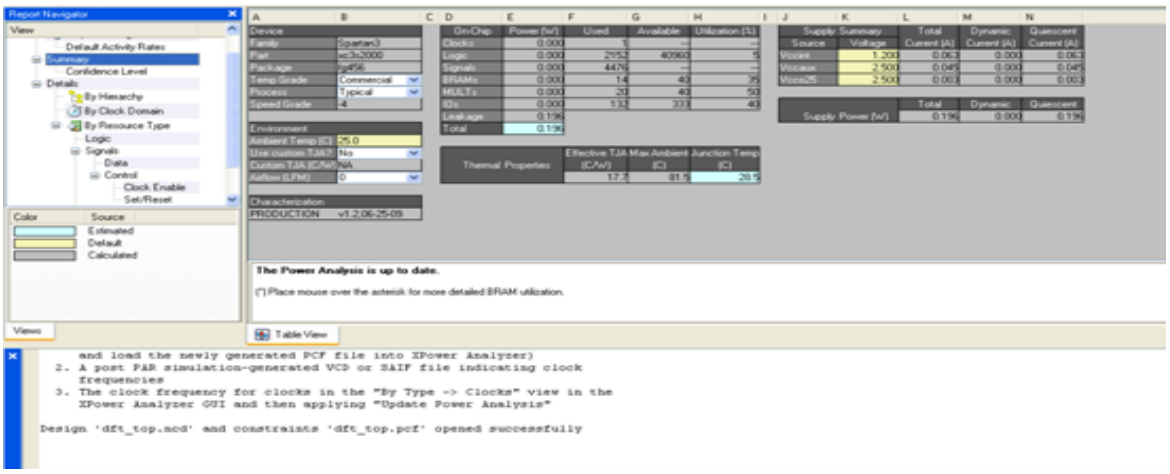

Figure 8: Power analysis result of FFT

The above figure shows the power analysis result of FFT using ALU. Result shows that the amount of power required is less than the DIT method.

5. Conclusion

A novel 8-point FFT and 64-point FFT design using ALU was described. The proposed architecture gives an advantage in terms of power and area compared with the design of FFT using Decimation in Time butterfly structure. The FFT design using ALU is more efficient compared to the previous method. The simulation results shows that the proposed architecture significantly reduces the number of operations inside the FFT compared with the DIT method. The proposed processor can be integrated with other components to be used as stand-alone processor applied for wireless communication systems.

6. Future Work

The FFT is implemented using Arithmetic Logic Unit (ALU) that consist of ripple carry adder, subtractor and normal multiplier. In future the normal multiplier is replaced by vedic multiplier for the design of FFT. Also the IFFT will design using the ALU block for the efficient implementation of OFDM transceiver block.

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