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BOEMDET-Band Offsets and Effective Mass Determination Technique applied to MIS devices on silicon to obtain the unknown bandgap of insulators.

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Abstract: *The Fowler-Nordheim carrier tunneling slope constants for electron and hole conduction through MOS devices fabricated on silicon substrate can be utilized to determine the conduction and valence band offsets, carrier effective masses in the* SiO_2 *and its unknown bandgap, independent of photoemission spectroscopic measurements of band offsets on* SiO_2*/Si samples. The slope constants can be obtained from the electron and hole tunneling currents versus oxide voltage characteristics on a pair of n-MOS and p-MOS devices in accumulation. This characterization technique called BOEMDET, can be applied to other insulating materials grown or deposited on silicon, such as jet vapor deposited (JVD) nitride, HfSiON,* SiO_xN_y*, AlN, BN, high-K oxides, and transparent conducting oxides (TCO).*
Keywords: *effective mass, FN-tunneling, band offsets, metal-insulator-semiconductor*

I. Introduction

High dielectric constant oxides are viable candidates for metal-insulator-semiconductor (MIS) devices that can allow thicker layers to limit leakage current in the off state through the devices. The thicker layers can at the same time provide the same insulator capacitance per unit area as that of a thin layer of SiO_2 which has a low relative dielectric constant K of 3.9. The list of the viable oxide materials is provided in two recent reviews [1, 2]. The reviews describe research on various material issues pertaining to dielectric material for CMOS applications. The conduction through these dielectrics at high fields greater than 8MV/cm is described by the Fowler-Nordheim (FN) tunneling mechanism [3-6]. They contain traps in the bulk that causes Poole-Frenkel conduction at intermediate oxide fields of 5-7 MV/cm [7, 8]. The traps in the oxide trap electrons under voltage or current stress and shift the threshold voltage of the MOSFET device [9]. There is constant research into making these oxides amorphous and free of bulk traps to make them suitable as electronic materials. This causes reduction in the leakage current by about 10^4 times that in the SiO_2 at 1V for the same equivalent oxide thickness [2]. The process of making the amorphous films also causes change in K value, increase in the interface trap density, and addition of fixed charges [2]. Two suitable amorphous dielectric materials for CMOS applications are thermal SiO_2 and Jet Vapor Deposited (JVD) silicon nitride that exhibit only FN tunneling because of negligible bulk traps [10, 11]. In a MOS device, FN tunneling mechanism can be utilized to determine the conduction and valence band offsets with Si<100> surface, the electron and hole effective masses in SiO_2[6], and determination of the unknown bandgap of SiO_2. This is the subject of the present study. The FN tunneling slope constants are the only measured parameters that are proposed to be used to determine the above MOS device parameters. The study will facilitate simulation of FN tunneling through a MOS device at high fields, and consequently estimate its breakdown field strength and the onset field for FN tunneling in amorphous insulators with negligible bulk traps. This technique called BOEMDET, of characterizing an MIS structure is an alternative option to the photoemission spectroscopic measurements of band offsets and bandgap.

II. Theory

FN electron and hole tunneling has been observed in Si and SiC MOS devices and in organic light emitting diodes [3, 5, 12]. The FN equation models the current-voltage characteristics across a MOS device at high fields. It is given by the classical equation [4, 5]:

$$\frac{J}{E^2} = A\exp\left(\frac{-B}{E}\right)......(1);$$

where J is the current density across the MOS device in A/cm^2, E is the oxide electric field in V/cm, and the pre-exponent A and the slope constant B are given by:

$$A = \frac{e^3 m}{16\pi^2 \hbar m_{ox} \phi_0} \ldots\ldots(2)$$

$$A = 1.54x10^{-6} \frac{m}{m_{ox}} \frac{1}{\phi_0} \ldots\ldots(A/V^2)$$

$$B = \frac{4}{3} \frac{(2m_{ox})^{1/2}}{e\hbar} \phi_0^{3/2} \ldots\ldots(3)$$

$$B = 6.83x10^7 \left(\frac{m_{ox}}{m}\right)^{1/2} \phi_0^{3/2} \ldots\ldots(V/cm)$$

In A and B constants, e is the electronic charge, m is the free electron mass, m_{ox} is the electron or hole mass in the oxide, $2\pi\hbar$ is Planck's constant and ϕ_0 is the electron or hole barrier height expressed in electron volts. A plot of $\ln(J/E^2)$ versus 1/E, called an FN plot, gives the value of the slope constant B, from which $(m_{ox}/m)^{1/2}\phi_0^{3/2}$ product can be obtained. Then, with a known effective mass, ϕ_0 can be calculated, and with a known ϕ_0, the effective mass in the oxide can be calculated. The slope constant B is very sensitive to the oxide field as it is in the exponential and therefore precise determination of the oxide field is absolutely critical in the evaluation of the tunneling parameters. The $\ln(J/E^2)$ term is relatively much less sensitive to the oxide field as it is in the natural logarithm. The slope constant B can be independently used to determine the carrier effective masses, band offsets at the insulator-semiconductor surface and the insulator bandgap, without the knowledge of band offsets from photoemission spectroscopic measurements. This however is possible on the silicon substrate, where the grown or deposited dielectric film forms an abrupt interface and the intrinsic Fermi level of silicon lies very near the middle of its bandgap after the growth or deposition of the film due to negligible intrinsic defects in the silicon substrate. The slope constants for electron current B_e, and for the hole current B_h, can be obtained from the current-voltage characteristics on a pair of n-MOS and p-MOS devices in accumulation.

A. Average oxide voltage in MOS devices and the corrected slope constant B

A MOS device is a two-terminal device and therefore, one dominating current can be measured at a time when the device is biased in accumulation. For an n-MOS device with the semiconductor as cathode, the dominant electron tunneling current can be measured. For a p-MOS device with the semiconductor as the anode, the dominant hole tunneling current can be measured, provided the hole barrier from the silicon valence band to oxide valence band is less than the electron barrier at the metal gate cathode. This can be achieved in silicon p-MOS device by having p^+-polysilicon carbide as the gate electrode providing 6 eV valence electron barrier. The hole barrier of 4.6 eV at the anode will then become less to allow the dominant hole tunneling current through the device in accumulation. Thus a pair of n-MOS and p-MOS devices on silicon having p^+ - polysilicon carbide gates and same thickness oxide can provide electron current and hole current versus oxide voltage characteristics, from which the inter-related FN slope constants B_e and B_h can be obtained. The figure 1 below shows the n-MOS and p-MOS devices with poly-SiC gates in accumulation.

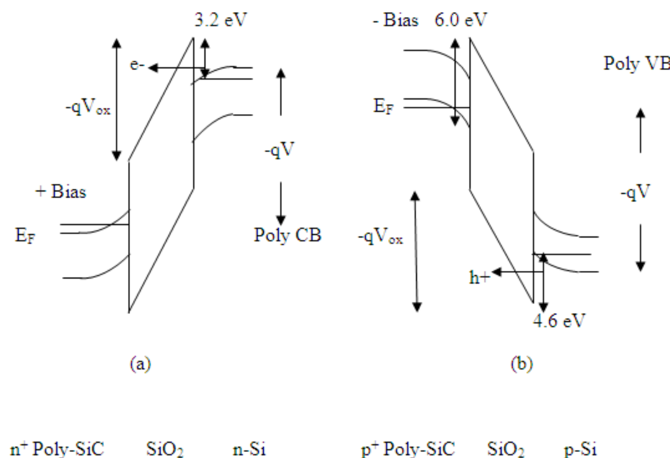

Fig. 1 Silicon MOS devices in accumulation: a) n-MOS and b) p-MOS with poly-SiC gates.

The formulation of the average oxide voltage in a pair of n-MOS and p-MOS devices is presented in the author's earlier report [6]. The formulae are presented here again and it is shown that the oxide voltage is corrected by the flatband voltage, V_{fb}, in MOS devices having thick oxides and metal gates. For a n-MOS device in accumulation and having positive charges or negative V_{fb}, and electron tunneling as the dominant current, the V_{ox} is given as,\

$$V_{ox} = |V_{app}| - |V_{fb}| \ldots\ldots(4);$$

where, V_{app} is the applied voltage across the device. This is the case in Si technology, where the charges in the gate oxide is generally positive and the metal-semiconductor work function difference, W_{ms}, exists as part of V_{fb} obtained from the capacitance-voltage characteristics [6]. For the oxide with net negative charges or positive V_{fb}, the oxide voltage is given as:

$$V_{ox} = |V_{app}| + |V_{fb}| \ldots\ldots(5) .$$

In case of hole tunneling as the dominant current in a p-MOS device in accumulation, the oxide having positive charges or negative V_{fb} will have V_{ox} as:

$$V_{ox} = |V_{app}| + |V_{fb}| \ldots\ldots(6) ,$$

and the oxide having net negative charges or positive V_{fb}, the oxide voltage is given as;

$$V_{ox} = |V_{app}| - |V_{fb}| \ldots\ldots(7).$$

In MOS devices having very thin oxide of less than 10nm and polysilicon carbide gates, the oxide voltage may have to be corrected by silicon surface band bending in accumulation and polysilicon carbide depletion potentials [6]. This is elaborated next.

For a MOS device in accumulation, the applied gate voltage is given as:

$$V_g = V_{fb} + V_{ox} + V_{sa} + V_p \cdots\cdots(8)$$

Here, V_g is the gate voltage, V_{fb} is the flatband voltage, V_{sa} is the silicon surface band bending in accumulation and V_p is the polysilicon carbide depletion potential drop. For a n-MOS device in accumulation, the gate voltage is positive and therefore the voltage drops V_{ox}, V_{sa}, and V_p are also positive. For a p-MOS device in accumulation, the gate voltage is negative and therefore the voltage drops V_{ox}, V_{sa} and V_p are also negative. V_{fb} could be positive or negative for both the devices. Equation (8) gives the oxide voltage as:

$$V_{ox} = V_g - (V_{fb} + V_{sa} + V_p)\cdots\cdots(9)$$

First, consider the expression (V_{fb} + V_{sa} + V_p) in equation (9) and analyze the effect of the individual terms on the charges at the gate. We know that for a MOS device,

$$V_{fb} = W_{ms} - \frac{Q_f}{C_i}\cdots\cdots(10)$$

where, Q_f is the density of fixed charges in Coul/cm^2 in the oxide and C_i is the insulator capacitance in F /cm^2. The effect of V_{fb}, particularly Q_f, on the cathode and anode field is studied earlier [6]. If the Q_f/C_i is made negligibly small as in case of the Si technology, then $V_{fb} = W_{ms}$, and the effect of only the W_{ms} can now be studied. If W_{ms} is negative in a MOS structure, then the positive charges are added to the metal when their Fermi levels try to align. Then, to achieve flat-band, negative voltage needs to be applied equal to W_{ms}. This negative voltage becomes positive due to the negative sign outside the expression in equation (9), implying that positive charges are added to the gate along with the gate voltage to obtain the oxide voltage. If W_{ms} is positive in the MOS structure, then negative charges are added to the gate when their Fermi levels try to align. Then, to achieve flat-band, positive voltage is applied to the gate equal to W_{ms}. This positive voltage becomes negative due to the negative sign outside the expression in equation (9), implying that negative charges are added to the gate along with the gate voltage to obtain the oxide voltage. V_{sa} and V_p are positive voltage drops for the n-MOS device, which imply addition of negative charges to the gate due to the negative sign outside the expression in equation (9) along with the gate voltage. V_{sa} and V_p are negative voltage drops for the p-MOS device, which imply addition of positive charges to the gate due to the negative sign outside the expression in equation (9) along with the gate voltage.

Now, consider equation (9) for the oxide voltage. If the expression (V_{fb} + V_{sa} + V_p) is negative, then positive charges are present at the gate along with the gate voltage due to the negative sign outside the expression in equation (9) to obtain the oxide voltage. These charges then enhance the field at the cathode for electron tunneling in a n-MOS device in accumulation. The true voltage across the oxide without charges will then be given as:

$$V_{ox} = |V_g| - |(V_{fb} + V_{sa} + V_p)|\cdots\cdots(11)$$

The oxide voltage with charges will then be equal to V_g, the same as in an ideal oxide. Here, if V_p and V_{sa} are neglected because of use of thick oxide greater than 10nm when the applied gate voltages are large, then the equation (11) reduces to equation (4) with V_{app} same as V_g. If the expression ($V_{fb}+V_{sa}+V_p$) is positive, then it implies that net negative charges are present at the gate along with the gate voltage due to the negative sign outside the expression in equation (9) to obtain the oxide voltage. These charges then reduce the field at the cathode for electron tunneling in a n-MOS device in accumulation. The true voltage across the oxide without charges will then be given as:

$$V_{ox} = \left|V_g\right| + \left|\left(V_{fb} + V_{sa} + V_p\right)\right| \cdots\cdots (12)$$

The oxide voltage with charges will then be equal to V_g, the same as in an ideal oxide. For negligible V_{sa} and V_p, equation (12) reduces to equation (5) with V_{app} same as V_g.

A similar analysis will result in equations (6) and (7) for hole tunneling from the anode in a p-MOS device in accumulation having negative voltage at the gate as shown in figure 1, resulting in negative voltage drops V_{ox}, V_{sa} and V_p in equation (8). If ($V_{fb}+V_{sa}+V_p$) is negative, then net positive charges are added to the gate along with the gate voltage due to the negative sign outside the expression in equation (9) to obtain the oxide voltage. This reduces the field at the anode for hole tunneling [6]. The true voltage of the oxide without charges will be given as:

$$V_{ox} = \left|V_g\right| + \left|(V_{fb} + V_{sa} + V_p)\right| \cdots\cdots (13)$$

The oxide voltage with charges will then be equal to V_g, the same as in an ideal oxide. For negligible V_{sa} and V_p for thick oxides greater than 10nm, equation (13) reduces to equation (6) with V_{app} same as V_g. If ($V_{fb}+V_{sa}+V_p$) is positive, then net negative charges are added to the gate along with the gate voltage due to the negative sign outside the expression in equation (9) to obtain the oxide voltage. This enhances the field at the anode for hole tunneling [6]. The true voltage of the oxide without charges will then be given as:

$$V_{ox} = \left|V_g\right| - \left|(V_{fb} + V_{sa} + V_p)\right| \cdots\cdots (14).$$

The oxide voltage with charges will then be equal to V_g, the same as in an ideal oxide. For negligible V_{sa} and V_p, equation (14) reduces to equation (7) with V_{app} same as V_g.

Equation (8) is also valid for a p-MOS device in inversion with positive gate voltage and a n-MOS device in inversion with negative gate voltage. In these devices also, the above analysis holds good with V_{sa} replaced by $V_{inv} = 2\ V_b$ with V_b as the bulk potential of silicon substrate. At V_{inv}, the MOS device attains the onset of strong inversion. The above analysis is not preferred for exact calculations of carrier effective masses or band offsets for a MOS device in inversion due to possible experimental errors described in the discussion section.

The corrected oxide voltages can be calculated as given in the above analysis. The slope constant B given in equation (3) is determined from the I-V characteristics using equation (1). First $\Delta\ln(J/E^2)/\Delta(1/E)$ is calculated by taking at least two points on the I-V characteristics in the FN regime at high fields utilizing the applied gate voltage. This yields the uncorrected B. Next, the corrected B is calculated by dividing $\Delta\ln(J/E^2)$ by$\Delta(1/E)$, with E obtained from the corrected oxide voltages corresponding to the same current density J as for the uncorrected B.

B. Modification of the FN slope constant equations for devices on silicon

It has been observed from a recent report of Ultraviolet photoemission and Inverse photoemission spectroscopic experiments on 2nm dry thermal SiO_2 [13], that the conduction and valence band offsets from the intrinsic silicon Fermi level are 3.8 eV and 5.1 eV respectively, and the bandgap of SiO_2 is 8.9 eV [13-15]. Taking the ratios of these values as 3.8/8.9 and 5.1/8.9 gives the electron and hole effective masses in the SiO_2 of 0.427m and 0.573m respectively. Within the experimental error of ±0.1 eV in the measurements of band offsets, the masses can be valued as 0.42m and 0.58m as reported earlier [6]. This ratio describes the ratio of the photo-emitted electron or hole kinetic energies during photoemission into the oxide conduction and valence bands as $\frac{0.5 m_{ox,e} v^2}{0.5(m_{ox,e}+m_{ox,h})v^2}$ which equals $\frac{m_{ox,e}}{m}$, thus giving the ratio of electron effective mass to the sum of electron and hole effective masses. Here, v is the drift velocity of the electron or hole in the oxide. The sum of the electron and hole effective masses equals the free electron mass for the amorphous insulators and therefore the band offsets to insulator bandgap ratio equals the relative carrier effective masses. Thus, the relative electron and hole effective masses $\frac{m_{ox,e}}{m}$ and $\frac{m_{ox,h}}{m}$ can be written as $\frac{(\phi_e + 0.55)}{E_g}$ and

$\frac{(\phi_h + 0.57)}{E_g}$ when the insulator is grown or deposited on Si<100> or Si<111> surface. Here, ϕ_e is the electron band offset from silicon conduction band to oxide conduction band and ϕ_h is the hole band offset from the silicon valence band to insulator valence band and 0.55 and 0.57 eV are added respectively to coincide the band offsets from the intrinsic Fermi level of silicon. The intrinsic Fermi level E_i of silicon is given by:

$$E_i = \frac{E_c + E_v}{2} + \frac{kT}{2} \ln\left[\frac{N_v}{N_c}\right] \ldots\ldots(15)$$

where E_c is the bottom of the conduction band, E_v is the top of the valence band, N_c is the effective density of states in the conduction band, and N_v is the effective density of states in the valence band. N_c for silicon equals 2.8 x $10^{19}/cm^3$ and N_v equals 1.04 x $10^{19}/cm^3$ at 300K temperature [16]. Evaluating the above equation gives the position of intrinsic Fermi level of silicon about 0.01 eV above the middle of the silicon bandgap. Thus 0.55 eV is added to ϕ_e and 0.57 eV is added to ϕ_h for the conduction and valence band offsets from the intrinsic Fermi level of silicon. If B_e and B_h are the electron and hole tunneling slope constants, then the slope constant equations can be written as below:

$$B_e = 6.83x10^7 \left(\frac{m_{ox,e}}{m}\right)^{1/2} \phi_e^{3/2} \ldots(16)$$

$$B_h = 6.83x10^7 \left(\frac{m_{ox,h}}{m}\right)^{1/2} \phi_h^{3/2} \ldots(17)$$

Substituting for $\frac{m_{ox,e}}{m}$ and $\frac{m_{ox,h}}{m}$, the equations become

$$B_e = 6.83x10^7 \left(\frac{\phi_e + 0.55}{E_g}\right)^{1/2} \phi_e^{3/2} \ldots(18)$$

$$B_h = 6.83x10^7 \left(\frac{\phi_h + 0.57}{E_g}\right)^{1/2} \phi_h^{3/2} \ldots(19)$$

$$E_g = \phi_e + \phi_h + 1.12 \ldots\ldots(20)$$

The equations (18), (19), and (20) form three non-linear simultaneous equations with three unknowns that can be solved with a simple MATLAB software program or by trial and error for a given B_e and B_h values. This evaluation will result in the values of ϕ_e , ϕ_h and E_g. Following this evaluation, the band offsets from the intrinsic silicon Fermi level can be obtained. Further, the carrier effective masses and the unknown bandgap of the insulator can be determined. The character of an MIS structure can thus be described by the below mentioned Table I as:

ϕ_e	ϕ_h	E_g	m_e	m_h

III. Results and Discussion

The electron and hole effective masses in the different high-K oxides grown by the atomic layer deposition (ALD) , and which are viable for the MOS technology are calculated and presented in Table II below. These values are based on the Ultraviolet photoemission and Inverse photoemission spectroscopic measurements presented in reference [13].

Table II. The electron and hole effective masses in different high-K oxides

Oxide [Ref.]	Growth process and thickness in (nm)	ΔE_c from E_i (eV)	ΔE_v from E_i (eV)	Band gap E_g (eV)	Electron effective mass in oxide $\frac{m_{ox,e}}{m} = \frac{\Delta E_c}{E_g}$	Hole effective mass in oxide $\frac{m_{ox,h}}{m} = \frac{\Delta E_v}{E_g}$
HfO_2[13]	ALD, 1.5	2.4	3.3	5.7	0.42	0.58
$Hf_{0.7}Si_{0.3}O_2$ [13]	ALD, 1.5	2.6	3.4	6.0	0.43	0.57
ZrO_2 [13]	ALD, 2.4	2.2	3.3	5.5	0.40	0.60
Al_2O_3 [13]	ALD. 2.5	3.2	3.8	7.0	0.46	0.54
SiO_2 [17]	Remote Plasma, 1.0	-	5.1	8.9	-	0.573
SiO_2 [13]	Dry thermal,2.0	3.8	5.1	8.9	0.427	0.573

In the present study, only the B_e and B_h values have been proposed to be utilized to determine the band offsets and SiO_2 bandgap, and the electron and hole effective masses. The method proposed is different from the previous studies, where the literature value of the electron effective mass of 0.42m was utilized to determine the conduction band offset of 2.78 eV in SiO_2/4H-SiC<0001> sample [6]. Further, the photoemission bandgap measurement of 8.9 eV was utilized to determine the hole effective mass in the SiO_2 of 0.58m [6]. The FN technique based on the I-V/C-V measurements can be considered as an alternative option to the photoemission measurements. Further, since the tunneling distance in FN tunneling does not change appreciably due to Schottky barrier lowering [4], the FN technique can be supported to provide relatively more accurate measurement than the photoemission spectroscopy which has a resolution of ±0.1 eV . The FN technique has been demonstrated to give an error in the electron effective mass calculations of less than 4% [4]. The high-K oxides [1, 2, 13] found viable for the MOS technology shows Frenkel-Poole conduction at medium oxide fields of 5-7 MV/cm due to presence of bulk traps and Fowler-Nordheim conduction at high oxide fields greater than 8 MV/cm [7, 8]. Presently, the high-K oxides are grown by a wide variety of processing techniques such as chemical vapor deposition, e-beam evaporation, jet vapor deposition, atomic layer deposition, ion-beam sputtering, pulsed-laser deposition etc., and these oxides may exhibit varied conduction mechanisms before and after annealing. Ultimately, the objective is to remove the bulk traps by improved processing techniques to make the films amorphous and exhibit only FN tunneling as in thermal SiO_2 or JVD nitride. There is evidence that the HfO_2 films deposited by chemical vapor deposition method over a silicon oxynitride surface is amorphous and becomes polycrystalline after 600-800°C vacuum annealing and increases the leakage current by about three orders of magnitude [18]. Further vacuum anneal at a 1000°C for 10s completely reduces HfO_2 to $HfSi_x$ [19]. The conduction and valence band offsets and the carrier masses presented in Table II can help to simulate FN tunneling currents at high field region and estimate the breakdown strength of the films, or conversely, a given FN tunneling current-voltage characteristics at high fields on a high-K oxide film can be utilized to calculate the band offsets, bandgap and carrier mass values by the present technique. It is interesting to note at this point that the FN technique of MIS characterization is applicable to both the high-K oxides having direct tunneling oxide thickness and the oxide containing some bulk traps. This is because the FN tunneling is exhibited by both types of oxides at high oxide electric fields.

The electron and hole effective mass in 2nm thermal oxide are 0.42m and 0.58m as presented in Table II, keeping in view that the photoemission measurements have an error of ±0.1 eV in the measurements of band offsets. Earlier determination of electron effective mass of 0.42m for a 100nm thermal oxide [3] is also the same as those in the Table II for thinner SiO_2 films. The report of hole effective mass of 0.58m in 40 nm SiO_2 grown on 4H-SiC [6] provides another supporting evidence of the above values. Thus it can be safely concluded that for all thicknesses of the SiO_2 in which bulk silica characteristics are present, the electron and hole effective masses are the same as above.

The obtained electron and hole effective mass values of 0.42m and 0.58m in SiO_2 are for a free Fermi gas model of carriers at the emitting electrode. However, if quantum confinement of carriers is considered at the emitting electrode, where the conduction or valence band edge forms a triangular potential well when biased, then these values have to be corrected. Nearly 70% population of carriers is calculated to be residing at the ground state subband energy level in the potential well [20], which reduces the electron barrier to oxide conduction band by 0.2eV [4], and the hole barrier to oxide valence band by 0.16eV [21] in Si<100> MOS devices. The corrected electron and hole barrier heights due to quantum confinement results in the electron and hole effective masses in the thermal oxide to 0.51m and 0.65m respectively. It needs to be mentioned here that quantum confinement which causes bandgap broadening at the semiconductor-oxide interface and affects the carrier effective mass calculations, is valid for extremely thin channels in the MOSFETs of a few tens of angstroms. The peak of the electron concentration due to quantum confinement lie several angstroms away

from the Si/SiO_2 interface because the nature of the wave function of the ground state where most of the carriers reside is a half sine wave.

A rethink on the determination of electron and hole effective mass in SiO_2 utilizing a silicon n-channel MOSFET device [22, 23] results in the conclusion that it is incorrect to relate the hole conduction over the anode barrier to the oxide field [24], and will result in erroneous hole effective mass. The threshold voltage taken as 1.25 V in the previous studies [22, 23] is for a 50nm oxide, whereas the oxide in question is only 8.5nm thick. This is incorrect. Moreover, in an n-channel MOSFET providing gate tunneling electron current and substrate hole current due to carrier separation, the oxide voltage is the same for both the currents in the same device. Keeping the above in view, it is necessary for field-dependent Fowler-Nordheim tunneling to occur for both the carriers that causes drift of carriers in the oxide due to the electric field [5]. This can be achieved by utilizing a pair of n-MOS and p-MOS devices in accumulation [6]. In the present study, a p-MOS device on silicon with p^+-poly-SiC gate in accumulation is considered, which will allow dominant hole tunneling to occur. Further, for a polysilicon gated MOS device in strong inversion, the oxide thickness is complicated by the polysilicon and inversion capacitances in series with the physical oxide capacitance giving a larger electrical oxide thickness than the physical thickness due to quantum confinement and polysilicon depletion. These will also complicate the oxide field and consequently the carrier effective mass calculations. The oxide voltage for MOSFET device is also shown to be different from the oxide voltage for a MOS device, particularly in MOSFETs having direct tunneling oxide thicknesses of 4nm or less [25].

Some applications that emerge from the use of BOEMDET technique are:

1. The conduction and valence band offsets and the unknown bandgap of an insulator or a wide band gap semiconducting material can be obtained.
2. The electron and hole effective masses in the insulator can be determined.
3. The dielectric breakdown electric field strength of the insulator can be estimated at a current density of 10^{-4} A/cm^2.
4. The electron and hole trap density in an insulator can be determined from the IV/CV measurements on the MIS devices on silicon.
5. The erase function in a FLASH memory can be performed by hole tunneling from the anode in a memory device where the electron barrier for the floating gate is more than the hole barrier at the anode.
6. Dielectric reliability studies due to electron and hole trapping under current and voltage stress can be studied.

IV. Conclusion

The present article proposes that a unique set of band offsets, unknown bandgap of the oxide, and the carrier masses in the oxide can be calculated from only the FN tunneling slope constant values obtained from MOS devices on silicon. This technique called BOEMDET, described in the present study can be utilized to characterize an MIS structure with different insulators. Once characterized, the parameters can be used to simulate the current-voltage characteristics and estimate the dielectric breakdown fields in the insulators. Also, the characteristics of two different MIS structures can be compared to give insight into relative reliability. The technique is considered to be an alternative option to photoemission spectroscopic measurements of band offsets and bandgap along with some more applications listed in the discussion.

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