Plasmon Talbot Masks For PN Junction Formation

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Abstract:

Plasmon Talbot masks for the fabrication of a pn-junction in a VLSI technique are presented. A completely interactive python program is reported for this purpose. The dimensions of the p- and n- regions can be controlled in the range 10nm to 100nm by suitably choosing the illuminating light source. The suggestive test diagram to realize the formation of the proposed Talbot masks is discussed.

Key Word: Plasmon, VLSI, pn-junction, fabrication, Talbot lithography, mask

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I. Introduction

Semiconductor fabrication techniques have been derived from the processes which were invented as back as 2000 years ago. The invention of lithography goes back to the year 1798 AD. At present, lithography represents more than 35% of the total IC manufacturing cost. Lithography includes: 1) the requirements of a clean room, 2) mask formation, 3) pattern transfer from the mask onto the wafer, 4) resists, 5) choice of light/radiation source of appropriate wavelength. Lithography offers many options including photo-lithography [1,2] electron beam lithography [3,4], extreme UV lithography [5], X-ray lithography [6,7], ion-beam lithography [8,9]. Correspondingly, the feature dimension has evolved from more than 10 µm during the early 1960 (small scale integration SSI) to a few nm as of today (ultra large scale integration ULSI). The requirement for further reducing the feature size and moving towards sub-nano technology, has encouraged the scientists and researchers to invent new lithography strategies including the emerging techniques such as employing Talbot effect to produce masks with sub nanometer feature dimensions and quantum lithography [10]. Talbot effect can further be studied employing "surface plasmon effect" [11,12,13]. In this research article, we propose the mask designing for the fabrication of a pn-junction, using Plasmon Talbot effect in a thin silver sheet.

II. Theory

The key concept is to employ a thin silver sheet of thickness of the order of 40nm-60nm (skin depth at optical frequencies) which has an array of holes along one of its axes. The diameter and the separation of the holes can be tailored to achieve the desired feature dimensions of the PN junction diode. Figure1 shows the schematic of the proximity lithographic technique. Figure2 displays the schematic of the silver plasmonic sheet with the array of holes shown in red colour. The illumination by the He-Ne laser is shown in yellow arrows. The half and full Talbot distances τ /2 and τ respectively are shown over the silver mask in yellow dotted lines. The flow chart to prepare this plasmonic mask is given in the next section. The output masks generated using the python program (Appendix I) are disclosed in Section IV (Figures 3 and 4). Details of the design parameters of the proposed masks are given in Table1. The feature dimensions obtained in these masks are listed in Table 2.

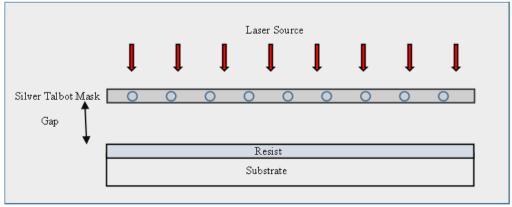


Fig.1: Schematic of the Proximity Lithographic Technique [14]

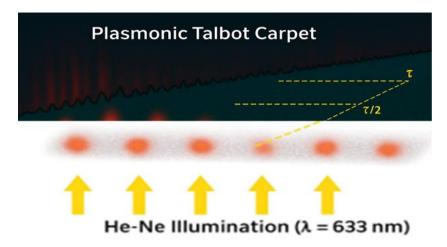
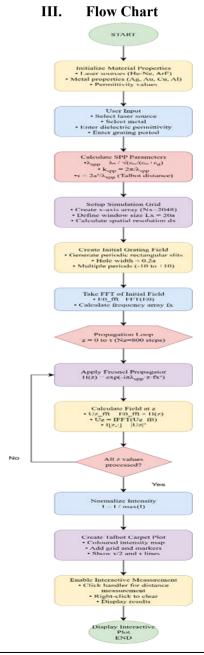


Fig.2: Schematic of the silver plasmonic sheet with the array of holes illuminated with He-Ne Laser



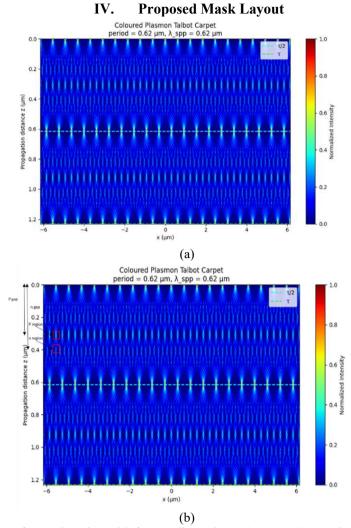
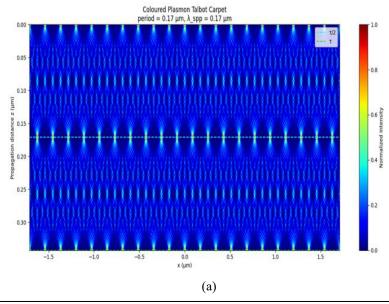


Fig. 3 a) Mask Layout for p-n junction with feature dimensions 40nm to 100nm using He-Ne Laser, b) mask with p- and n-regions marked and the p-gap and n-gap shown with arrows. The p-gap signifies the distance between the silver mask and the substrate during proximity printing when p-region is to be doped. Similarly the n-gap signifies the distance between the silver mask and the substrate during proximity printing when n-region is to be doped.



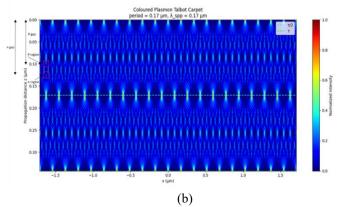


Fig. 4 a) Mask Layout for p-n junction with feature dimensions 10nm to 40nm using AF Laser, b) mask with p-and n-regions marked and the p-gap and n-gap shown with arrows. The p-gap signifies the distance between the silver mask and the substrate during proximity printing when p-region is to be doped. Similarly the n-gap signifies the distance between the silver mask and the substrate during proximity printing when n-region is to be doped.

Table1: Details of the design parameters of the proposed masks

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S.	Mask Layout	Light Source used	Separation	Hole diameter
No.	Preparation (Talbot		between holes	(0.2a)
	Length τ)		(a)	
1.	Mask 1(Fig. 3)	He-Ne	0.62μm	124nm
	(1.16µm)			
2.	Mask 2 (Fig. 4)	ArF	0.17μm	34nm
	$(0.34 \mu m)$			

Table2: Proposed Feature dimensions (in Figure 1) as obtained in the above proposed mask layouts using Plasmon Talbot effect.

S. No.	Light Source used	Width of Lower	Gap(See Fig2)	Width of Upper	Gap (see Fig2)
	-	Region (p region) d1		Region (n region) d2	
1.	He-Ne	40nm	30nm	100nm	40nm
2.	ArF	10nm	10nm	40nm	12.5nm

V. Conclusions And Discussion

The authors have reported plasmon masks for the fabrication of PN junction with feature dimensions 10nm to 100nm using the Plasmon Talbot effect. The work can be extended to design the masks for CMOS transistors which is the main technology being used these days in VLSI design.

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